

An Assembly primer

Guillaume DIDIER
L3 ENS - 2010/2021

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This lecture is fully preemptible
Feel free to interrupt with questions

Assembly / machine code view (ISA)

(user mode)

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CPU

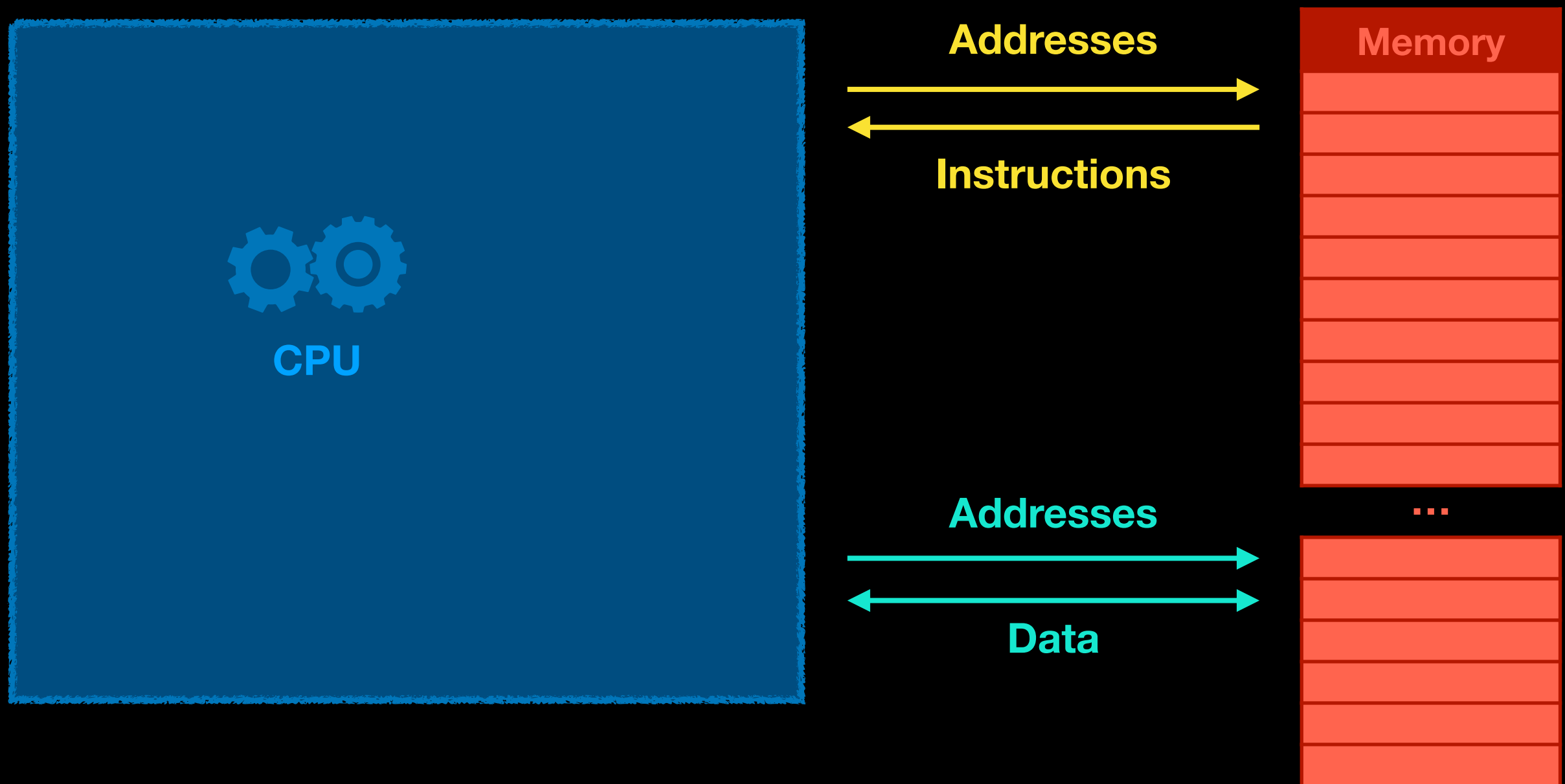
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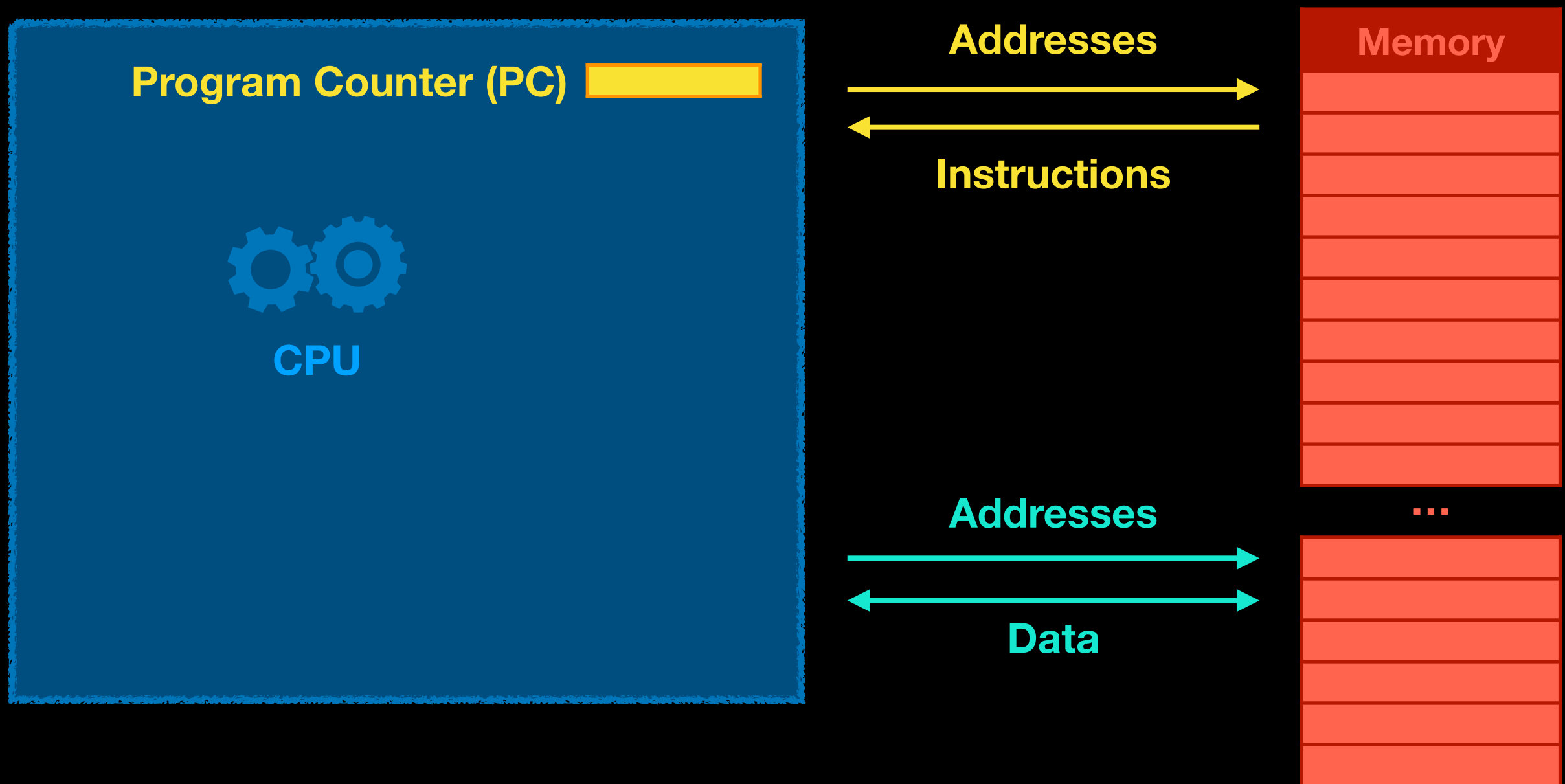
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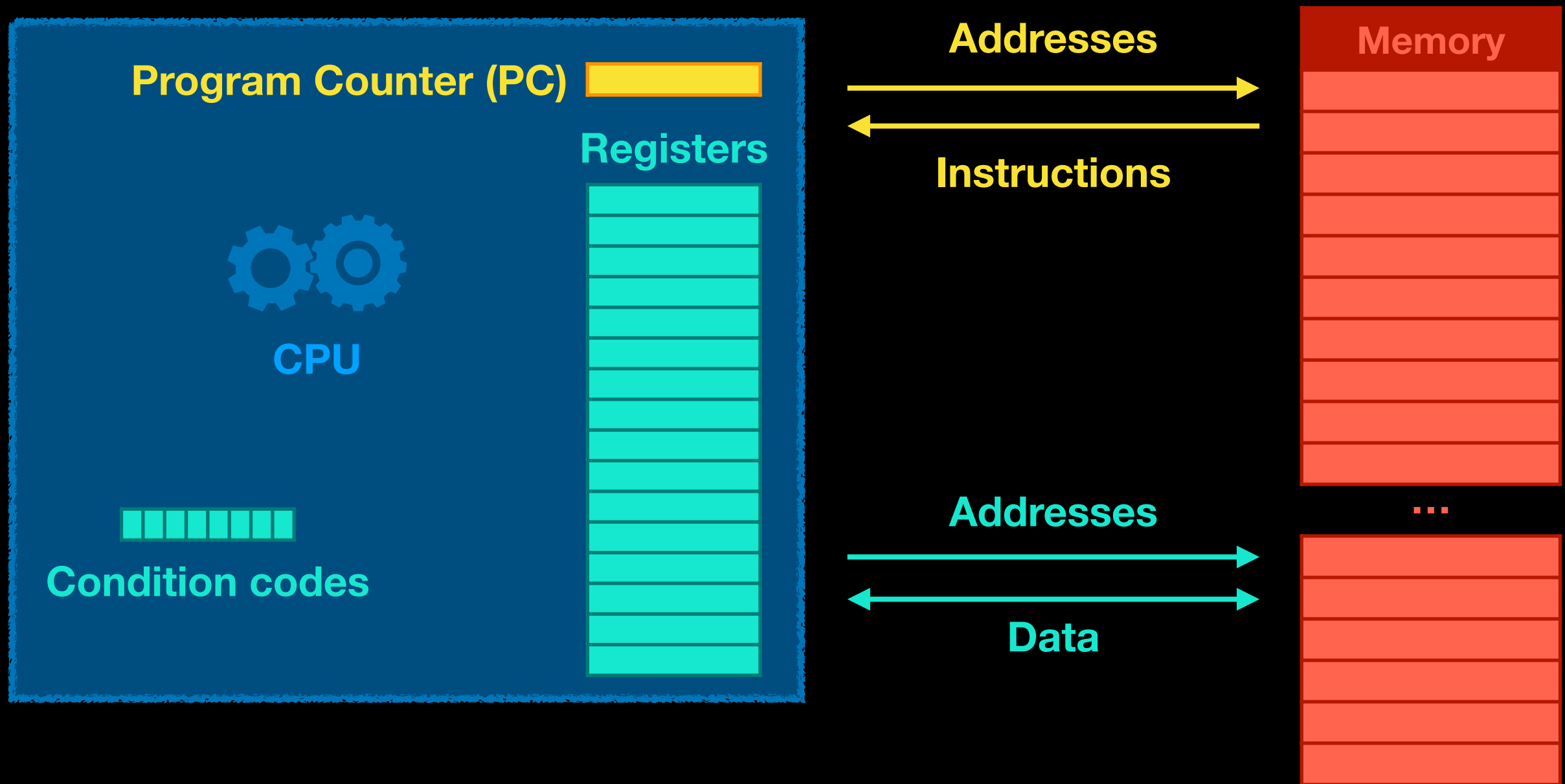
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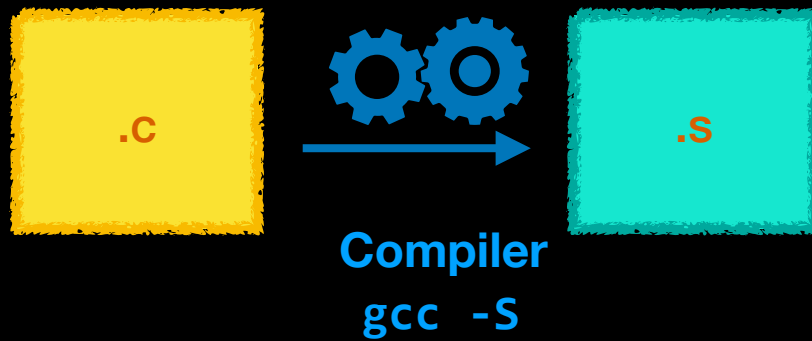
How to turn C code into a running process

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.c

```
long plus(long x, long y);  
void sumstore(long x, long y,  
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    long t = plus(x, y);  
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}
```

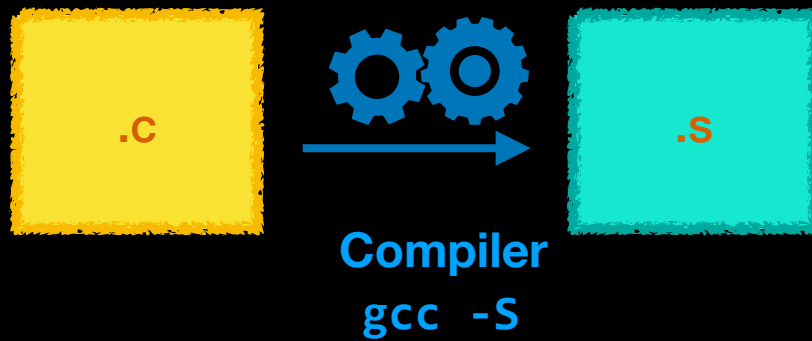
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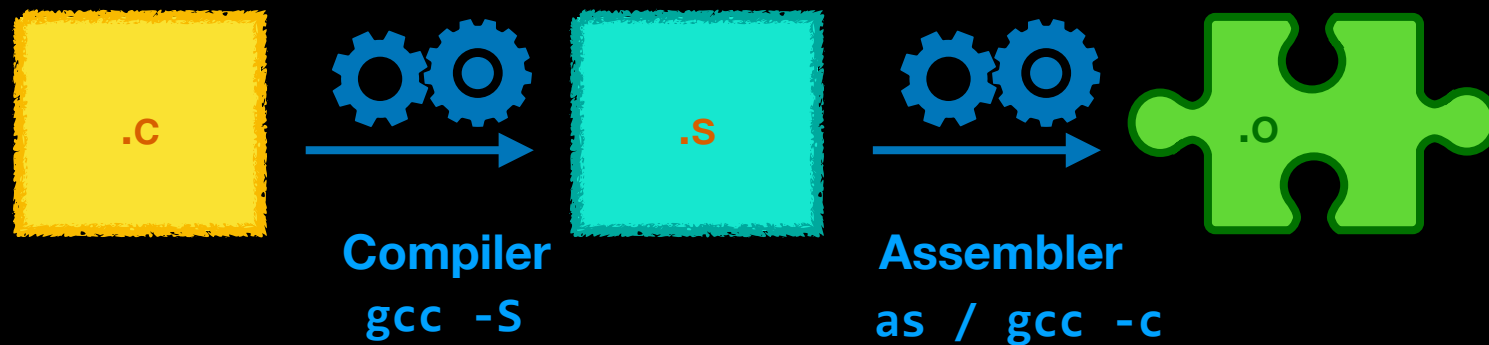
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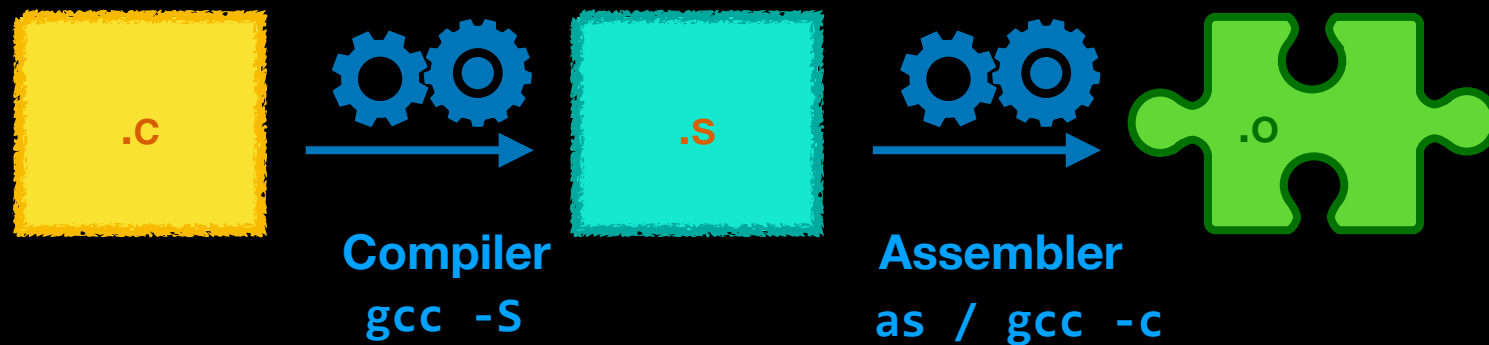
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How to turn C code into a running process

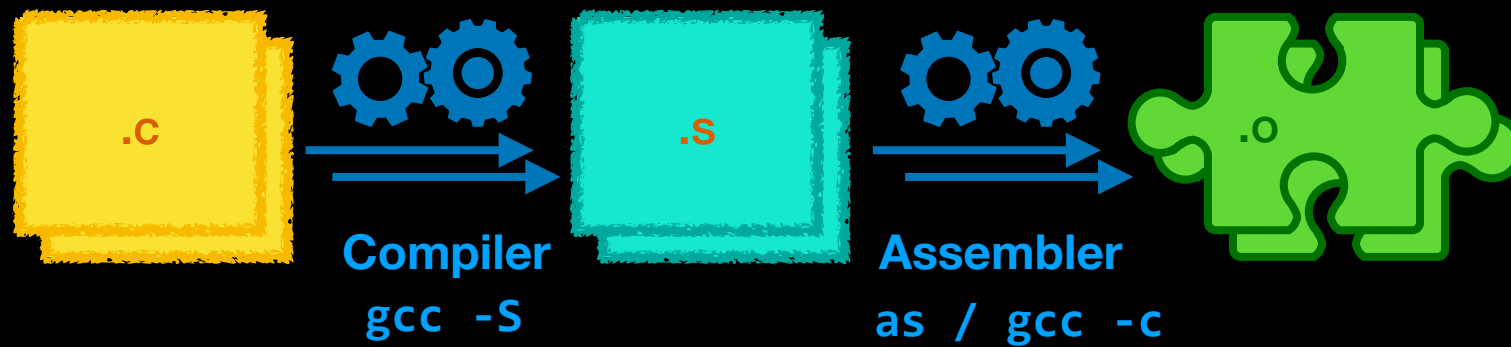


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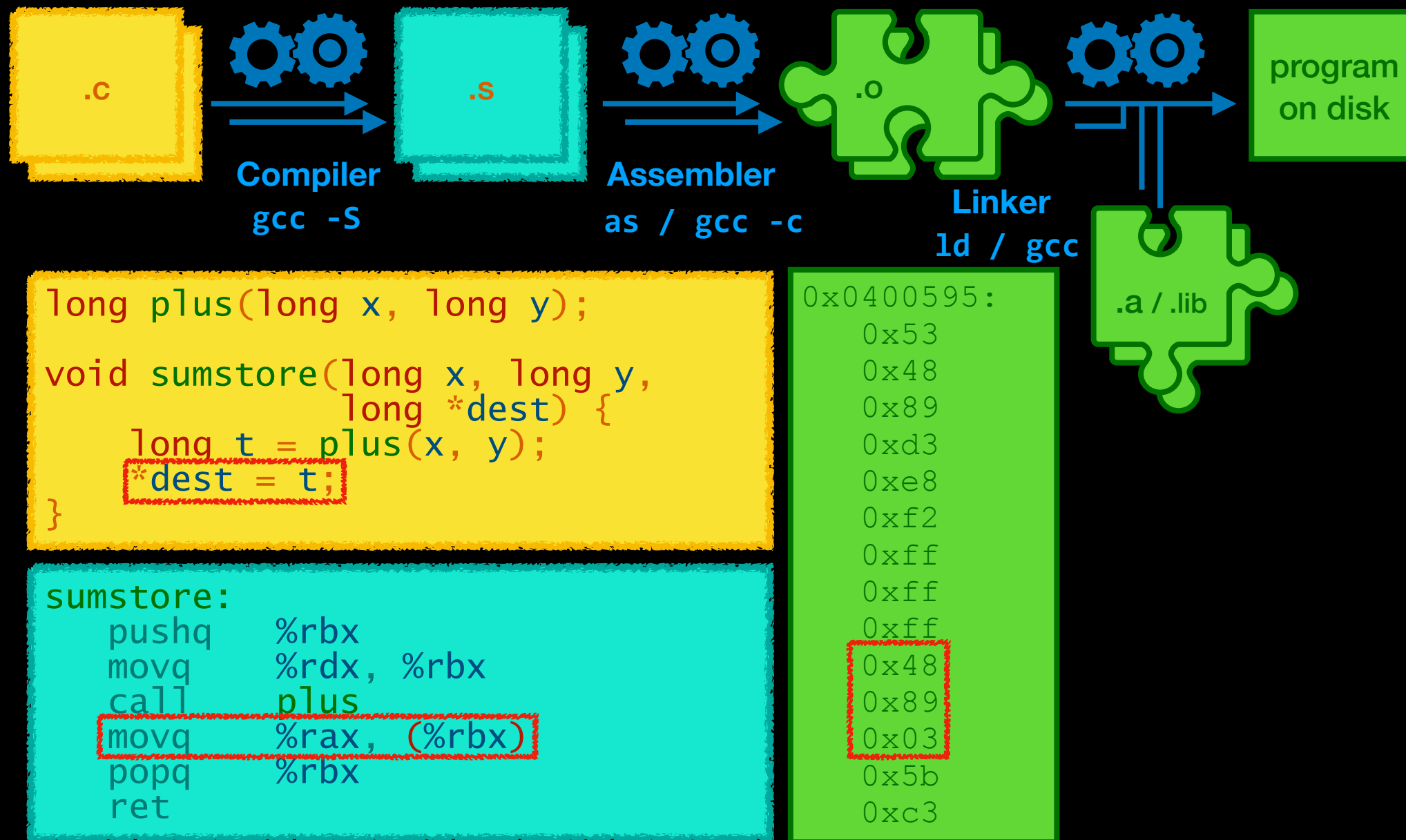


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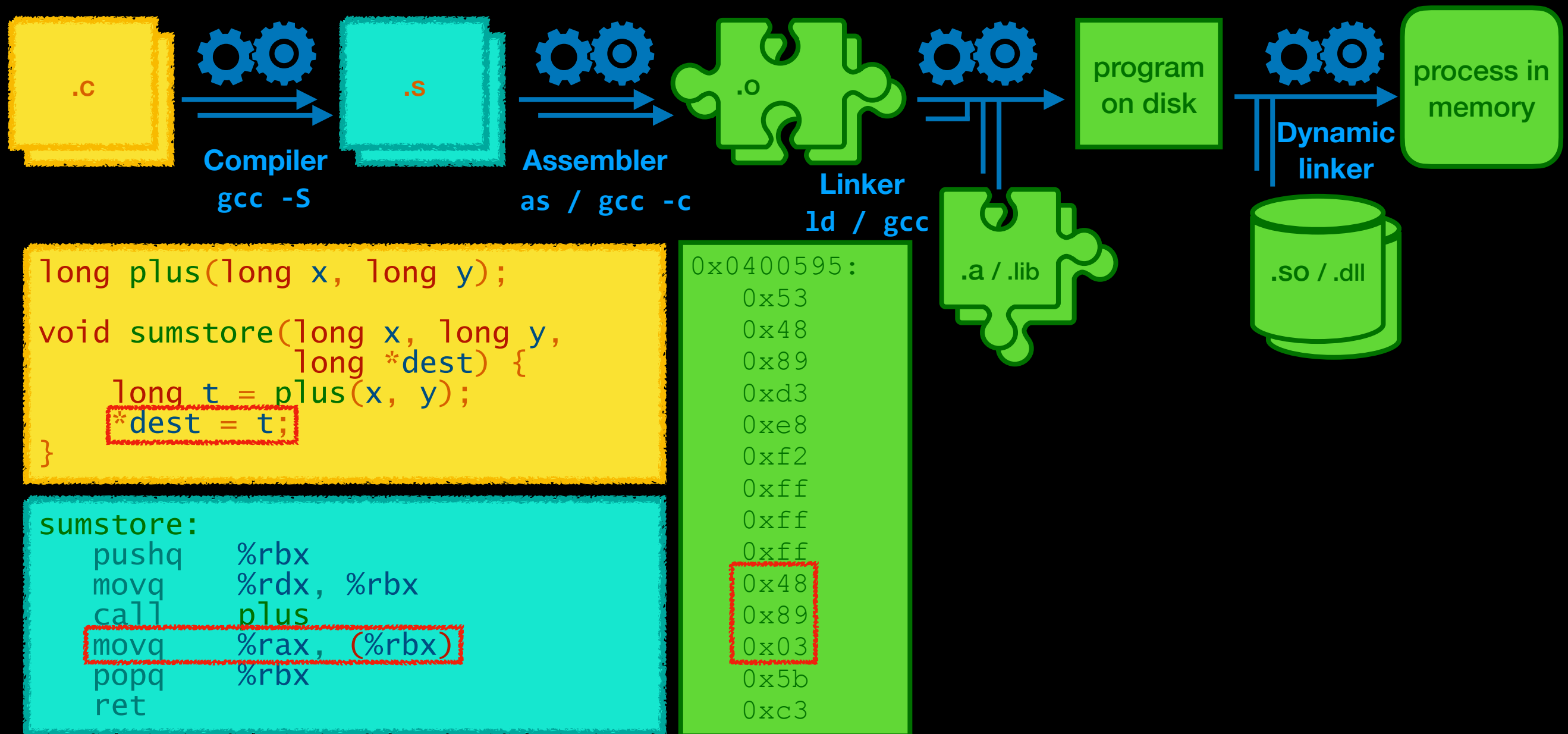
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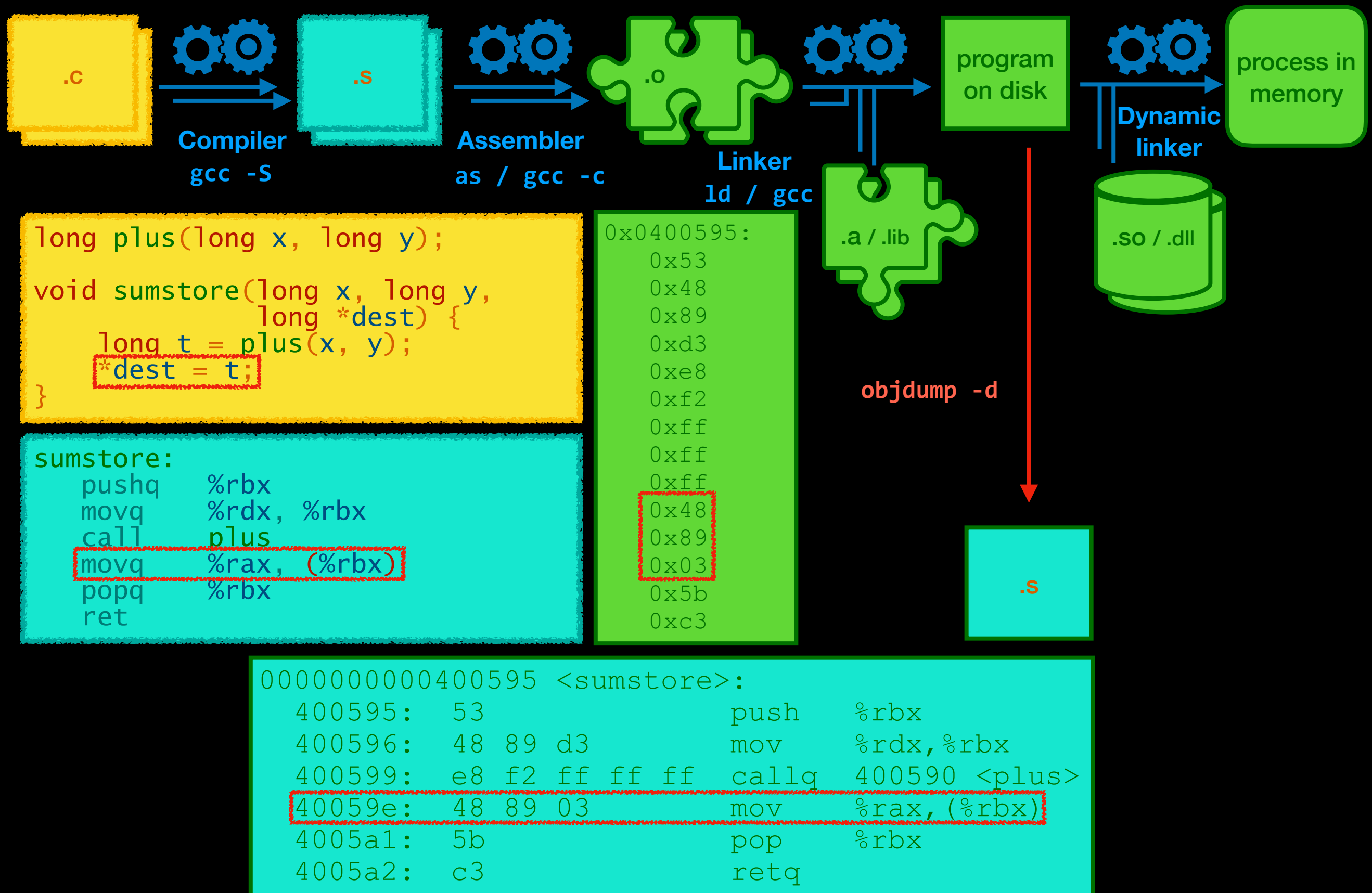
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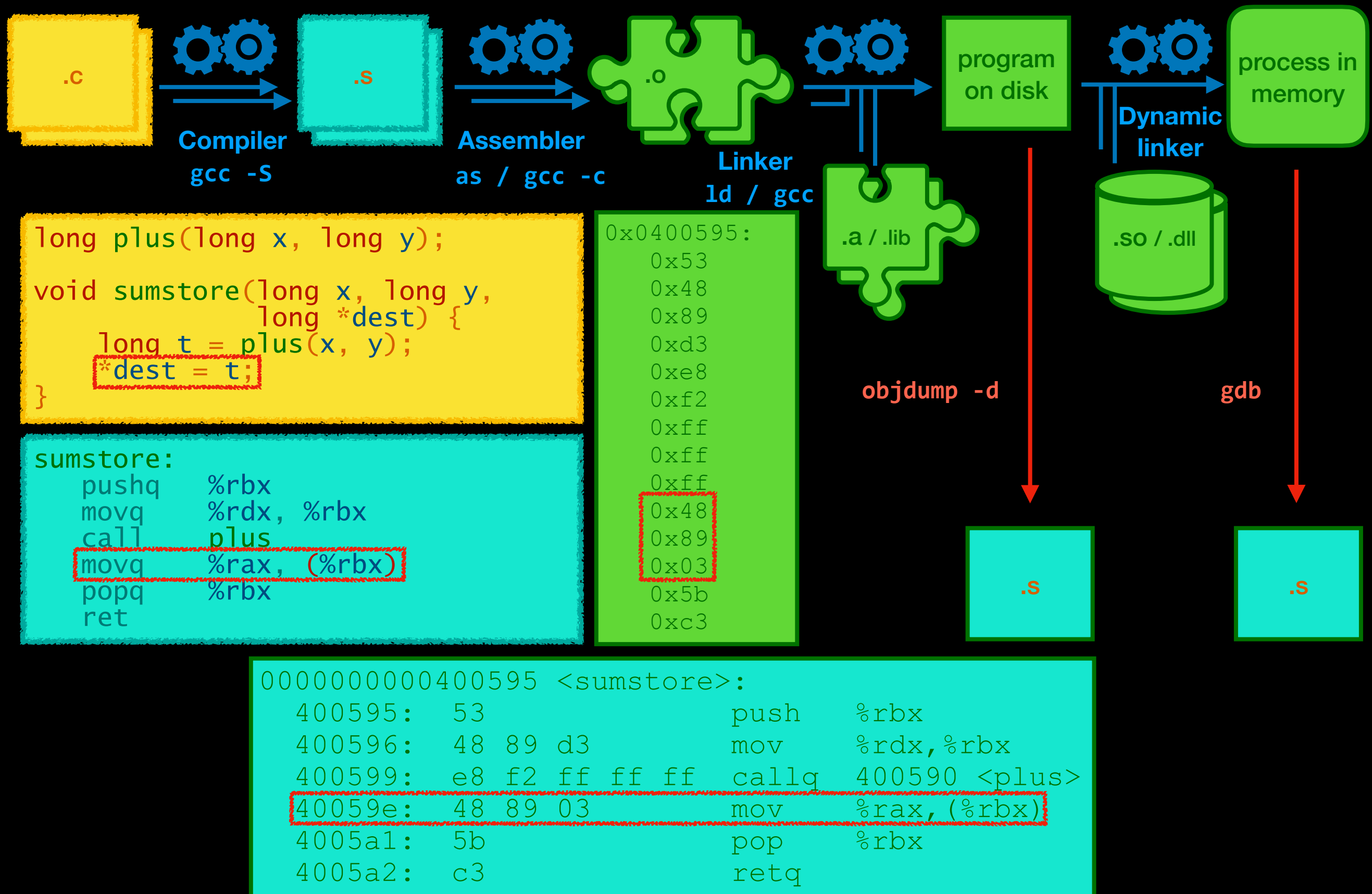
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How to turn C code into a running process



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- You may need it for your work!

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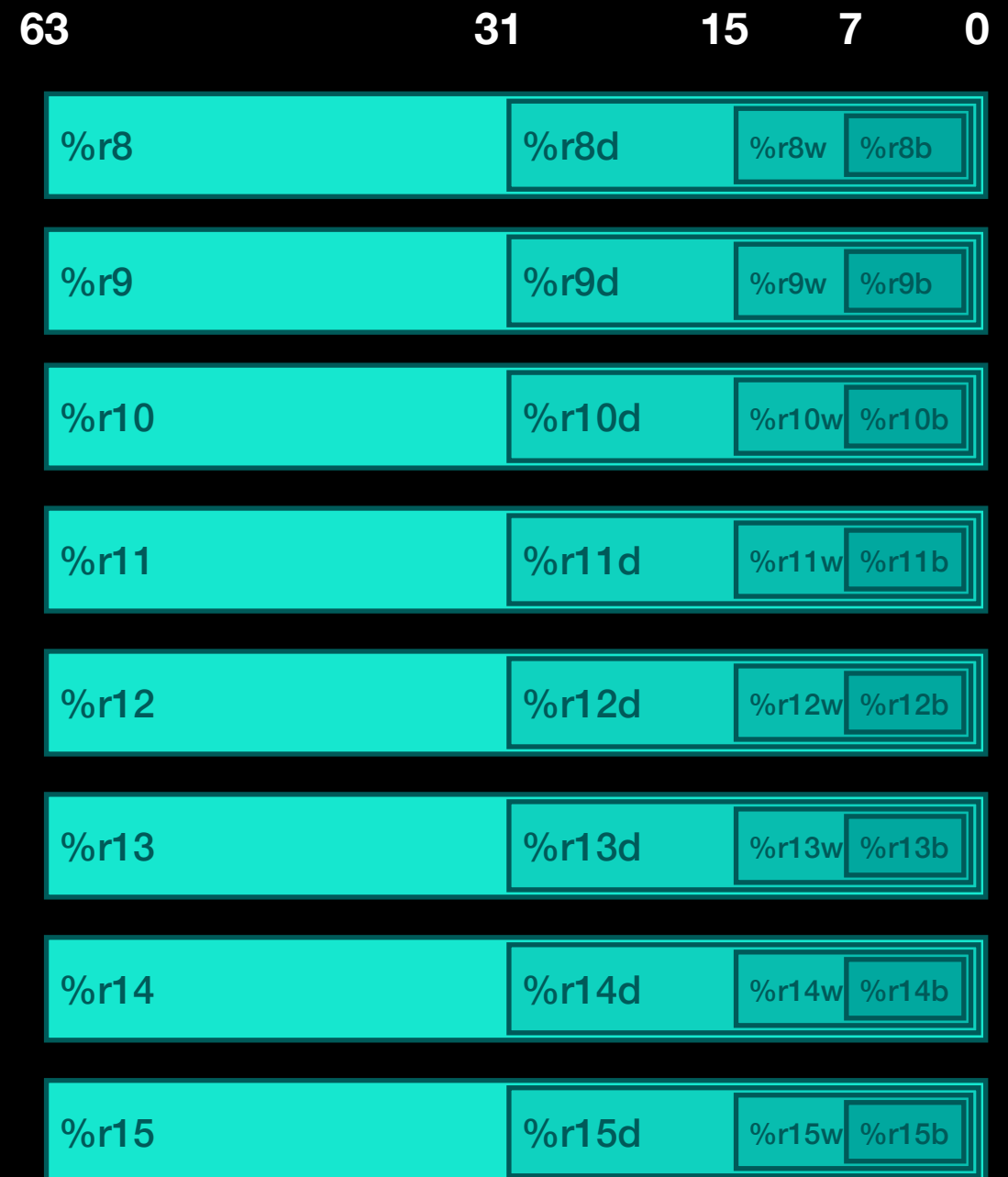
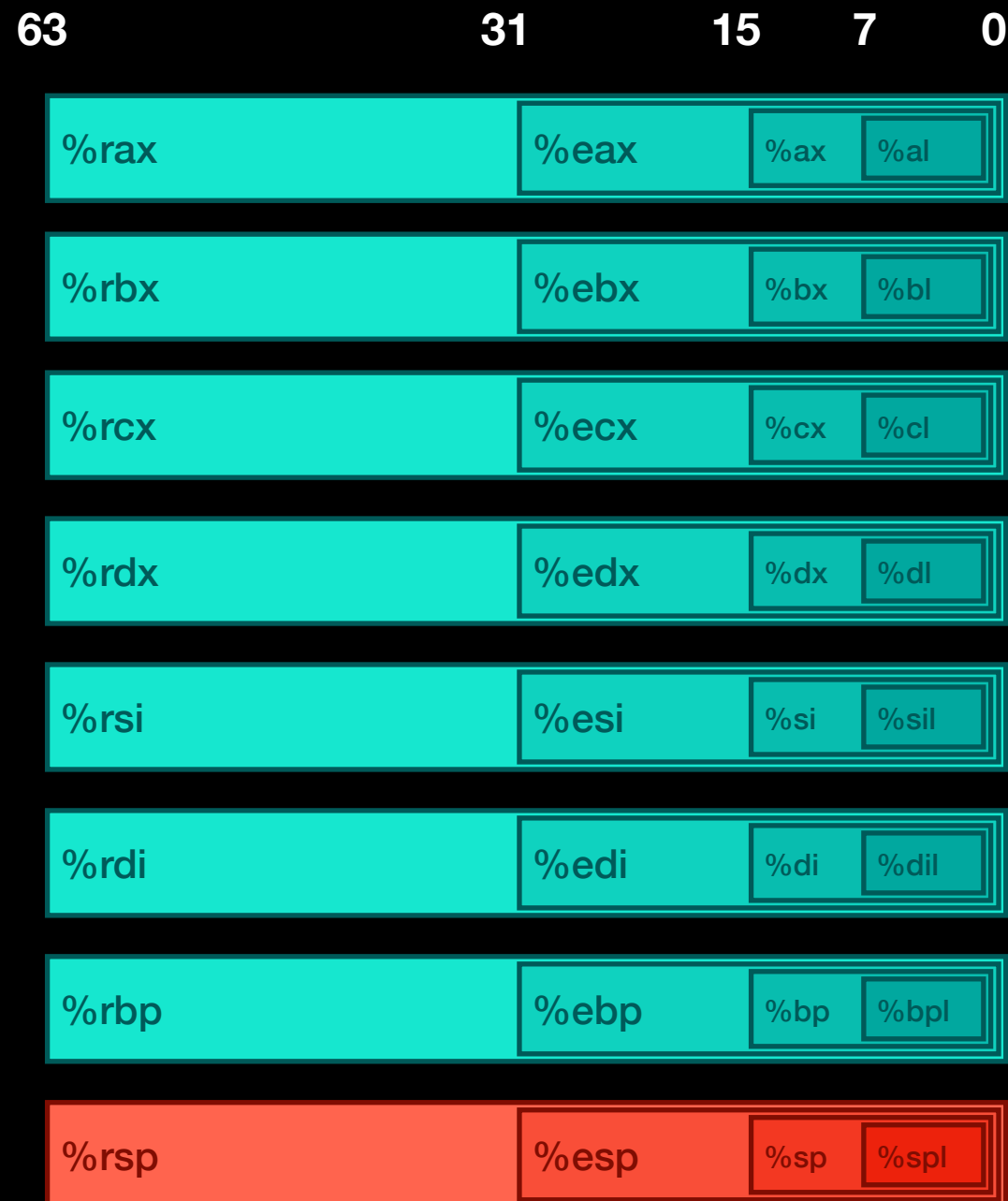
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- 1978 : birth of x86, Intel 8086 is a 16-bit micro processor
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- 2003 (AMD)-2004 (Intel) : 64-bit extension.
- *A lot of crufts left-over of x86 long and convoluted history.*

x86 has a long history

Registers

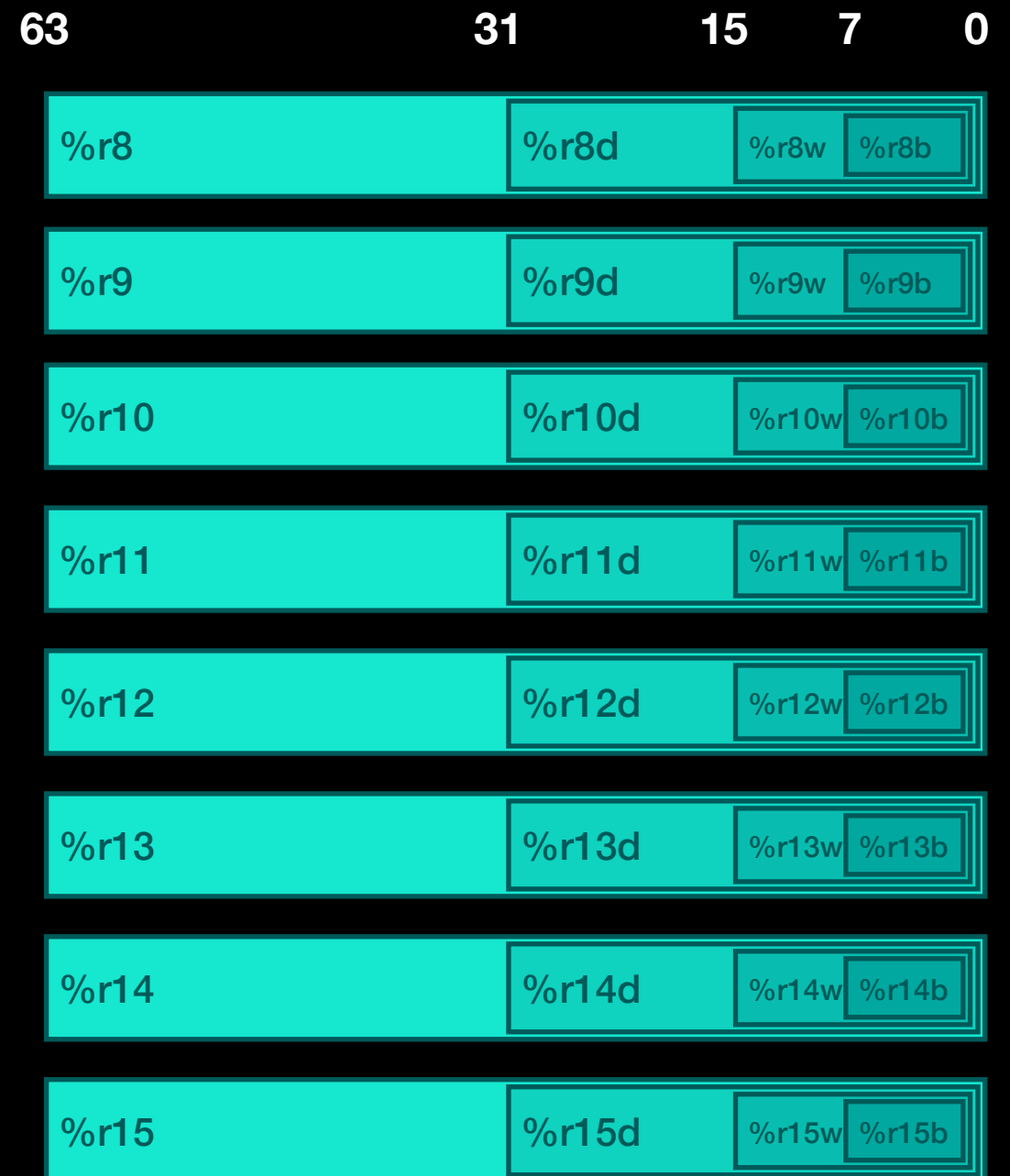
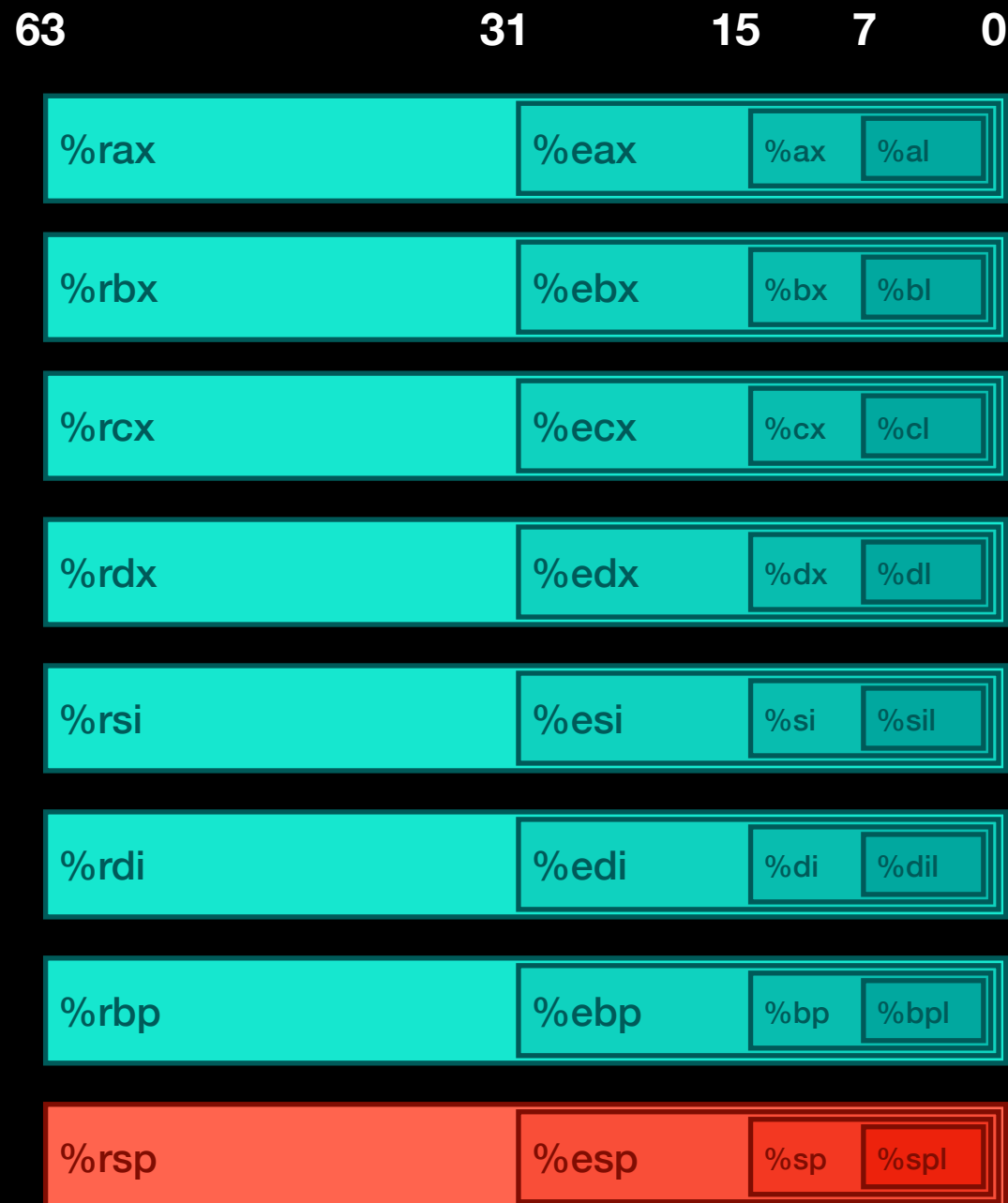
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- 16 registers, each 64 bits (8 bytes).



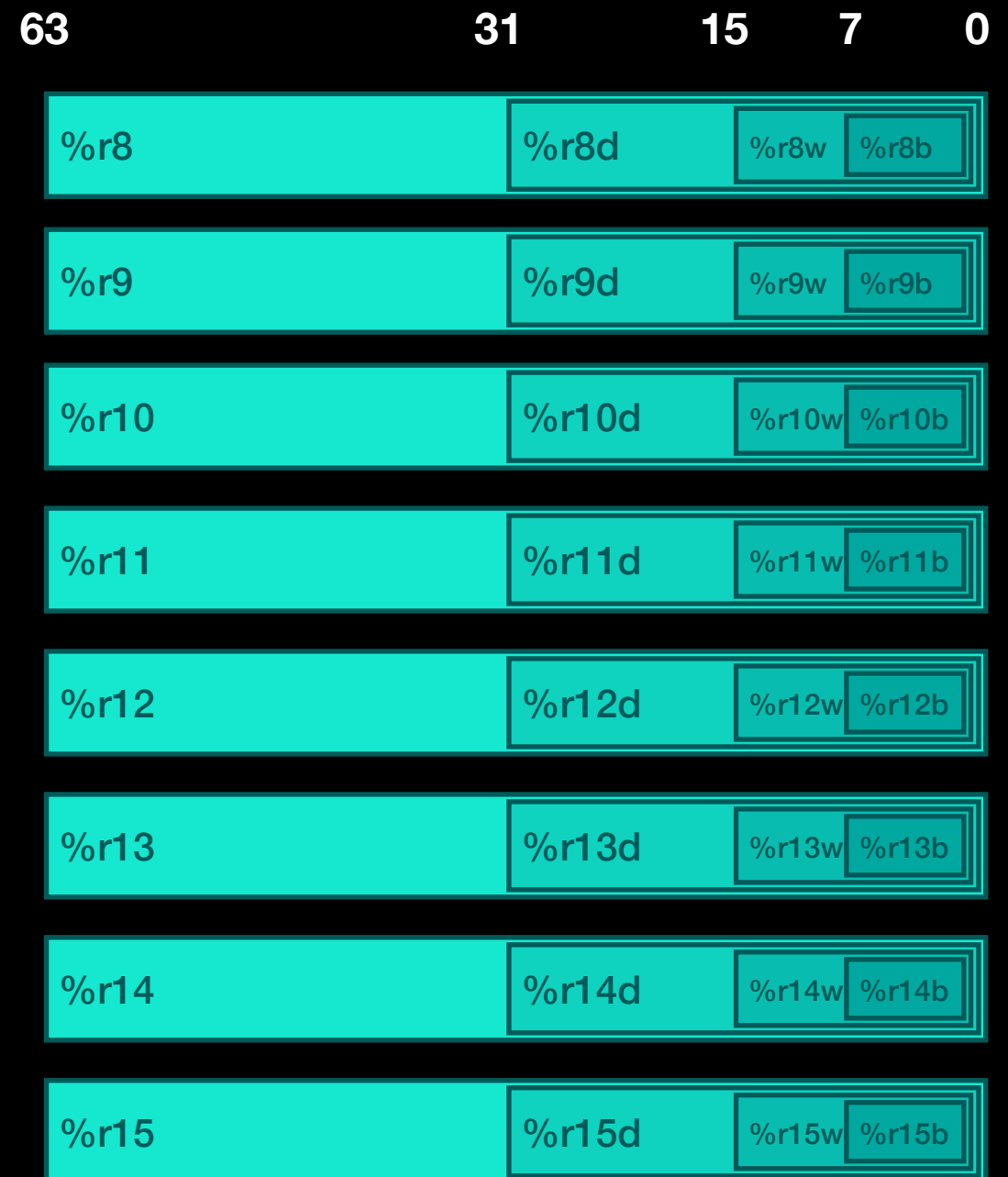
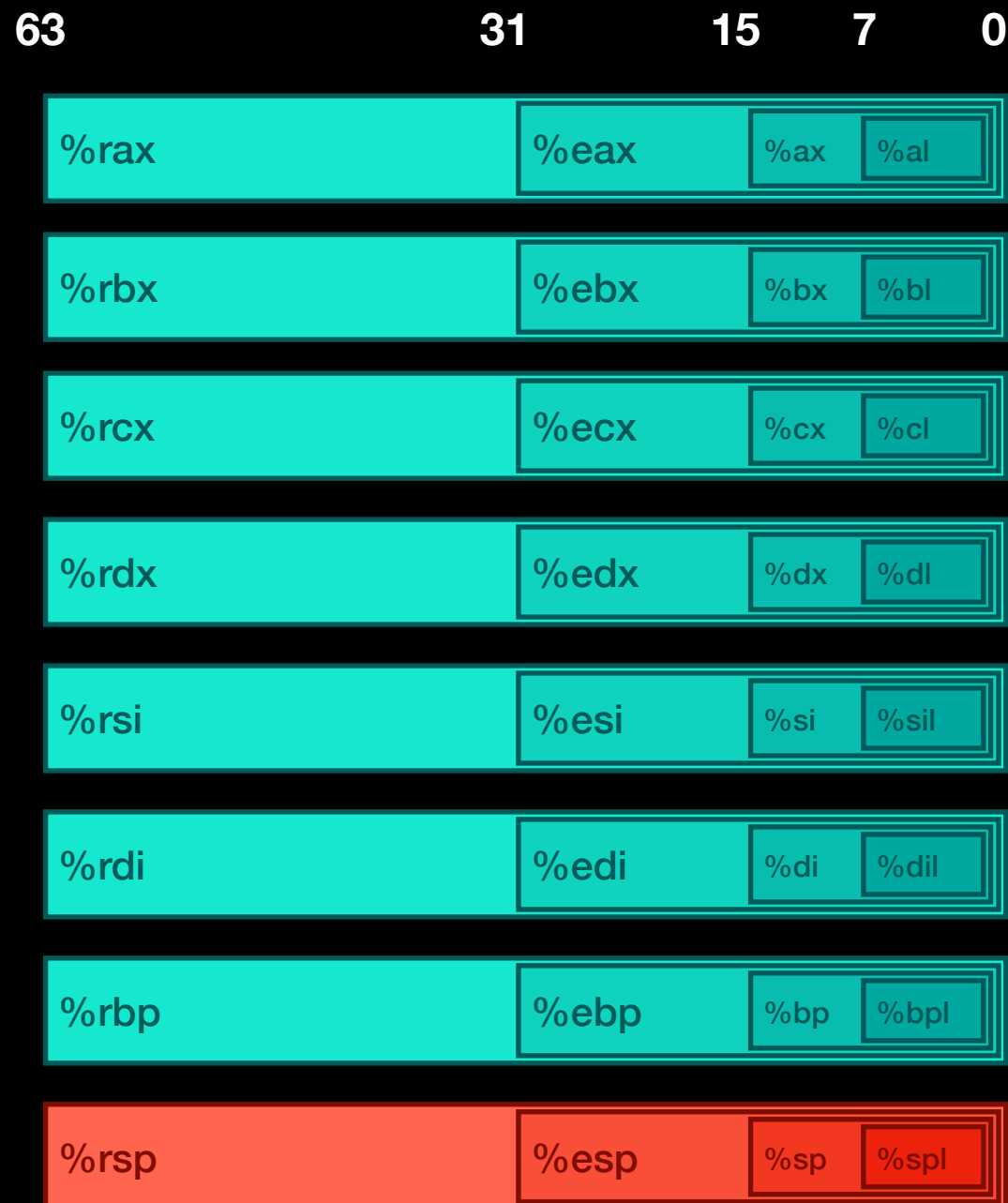
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- What the CPU mostly operates on.
- Suffixes on instructions used to make the size of operands explicit (can be omitted in some cases):
q, l, w, b, for resp. 8, 4, 2 and 1 bytes values



Assembler syntax

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In this presentation we exclusively use AT&T syntax.

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Cannot do memory-memory transfer in a single instruction

Example

Example

movq

Example

Source

Dest

Example

C analog

movq



Example

	Source	Dest	Example	C analog
movq	<i>Imm</i>	{ <i>Reg</i>	movq \$42, %rax	tmp = 42;

Example

	Source	Dest	Example	C analog
movq	Imm	Reg	movq \$42, %rax	tmp = 42;
		Mem	movq \$2020, (%rsp)	*year = 2020;

Example

	Source	Dest	Example	C analog
movq	Imm	Reg	movq \$42, %rax	tmp = 42;
		Mem	movq \$2020, (%rsp)	*year = 2020;
	Reg	Reg	movq %rdi, %rax	tmp2 = tmp1;

Example

	Source	Dest	Example	C analog
movq	Imm	Reg	movq \$42, %rax	tmp = 42;
		Mem	movq \$2020, (%rsp)	*year = 2020;
	Reg	Reg	movq %rdi, %rax	tmp2 = tmp1;
		Mem	movq %rax, (%rsi)	*p = tmp;

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void swap(long *xp, long *yp) {
    long t0 = *xp;
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movq	Imm	Reg	movq \$42, %rax	tmp = 42;
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```
swap:
    movq    (%rdi), %rax
    movq    (%rsi), %rdx
    movq    %rdx, (%rdi)
    movq    %rax, (%rsi)
    ret
```

Addressing modes

Addressing modes

- Most general form :
 $D(Rb, Ri, S)$: Refers to $addr = \text{Reg}[Rb] + \text{Reg}[Ri] * S + D$
 - D : Constant displacement encoded on 1,2 or 4 bytes
 - Rb : Base register: Any of the 16 integer registers
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- Any element can be omitted.
 - $0x48000$ - only D
 - $0x42(, \%rsi, 2)$ - Ri , S and D
 - $(\%rdi, \%rsi)$ - Rb and Ri ($S = 1$)

Arithmetic operations

Arithmetic operations

Instruction	Computation
<code>addq Src, Dest</code>	$\text{Dest} = \text{Dest} + \text{Src}$
<code>subq Src, Dest</code>	$\text{Dest} = \text{Dest} - \text{Src}$
<code>imul Src, Dest</code>	$\text{Dest} = \text{Dest} * \text{Src}$
<code>salq Src, Dest</code>	$\text{Dest} = \text{Dest} \ll \text{Src}$ Also known as <code>shlq</code>
<code>sarq Src, Dest</code>	$\text{Dest} = \text{Dest} \gg \text{Src}$ Arithmetic right shift
<code>shrq Src, Dest</code>	$\text{Dest} = \text{Dest} \gg \text{Src}$ Logical right shift
<code>xorq Src, Dest</code>	$\text{Dest} = \text{Dest} \wedge \text{Src}$
<code>andq Src, Dest</code>	$\text{Dest} = \text{Dest} \& \text{Src}$
<code>orq Src, Dest</code>	$\text{Dest} = \text{Dest} \text{Src}$
<code>incq Dest</code>	$\text{Dest} = \text{Dest} + 1$
<code>decq Dest</code>	$\text{Dest} = \text{Dest} - 1$
<code>negq Dest</code>	$\text{Dest} = -\text{Dest}$ Two complement
<code>notq Dest</code>	$\text{Dest} = \sim \text{Dest}$ Bitwise negation
...	<i>This is not an exhaustive list.</i>

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- Redirect the control flow elsewhere than the next instruction:
 - Define a *label* to jump to (`label:` before an instruction),
 - `jmpq label` will redirect execution to the label.
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    a = a + a;  
    while(1) {  
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```
loop:  
    addq    %rdi, %rdi  
while:  
    addq    $1, %rdi  
    jmpq    while
```

Condition codes

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Flag	Name	When is it set
CF	Carry flag	Arithmetic operation generates a carry or a borrow out of the MS bit
PF	Parity flag	LS byte of the result contains an even number of 1 bits
OF	Overflow flag	two's-complement overflow <code>(a > 0 && b > 0 && t < 0) (a < 0 && b < 0 && t >= 0)</code>
SF	Sign flag	<code>t < 0</code> (as two complement signed)
ZF	Zero flag	<code>t == 0</code>

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example:

```
movq    $42, %rax
movq    $12, %rdx
cmpq    %rdx, %rax
setge    %al
```

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movq    $42, %rax
movq    $12, %rdx
cmpq    %rdx, %rax
setge    %al
# al is 1 as 42 >= 12
```

Branches

(conditional `jmp` `label`)

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Instruction	Condition	Flags
<code>jo</code>	overflow	OF = 1
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<code>jb</code> / <code>jnae</code>	below / not above or equal	CF = 1
<code>jnb</code> / <code>jae</code>	not below / above or equal	CF = 0
<code>je</code> / <code>jz</code>	equal / zero	ZF = 1
<code>jne</code> / <code>jnz</code>	not equal / zero	ZF = 0
<code>jbe</code> / <code>jna</code>	below or equal / not above	(CF OR ZF) = 1
<code>jnbbe</code> / <code>ja</code>	neither below nor equal / above	(CF OR ZF) = 0
<code>js</code>	sign	SF = 1
<code>jns</code>	no sign	SF = 0
<code>jp</code> / <code>jpe</code>	parity even	PF = 1
<code>jnp</code> / <code>jpo</code>	parity odd	PF = 0
<code>jnl</code> / <code>jnge</code>	less / not greater or equal	(SF XOR CF) = 1
<code>jnl</code> / <code>jge</code>	not less / greater or equal	(SF XOR CF) = 0
<code>jle</code> / <code>jng</code>	less or equal / not greater	((SF XOR OF) OR ZF) = 1
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<code>jb / jnae</code>	below / not above or equal	CF = 1	Below / Above refers to unsigned Less / Greater to 2 complement signed
<code>jnb / jae</code>	not below / above or equal	CF = 0	
<code>je / jz</code>	equal / zero	ZF = 1	
<code>jne / jnz</code>	not equal / zero	ZF = 0	
<code>jbe / jna</code>	below or equal / not above	(CF OR ZF) = 1	
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**Below / Above refers to unsigned
Less / Greater to 2 complement signed**

example:

```
movq $0, %rax
testq %rdi, %rdi
jz end
movq $42, %rax
```

end:

what will %rax contain ?

if else, switch case

if else, switch case

```
long absdiff(long x, long y) {  
    long result;  
    if (x > y)  
        result = x - y;  
    else  
        result = y - x;  
    return result;  
}
```

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x in %rdi,
y in %rsi,
result in %rax

```
absdiff:  
    cmpq %rsi, %rdi  
    # set flags for x-y  
    jle .L4  
    movq %rdi, %rax  
    subq %rsi, %rax  
    ret  
.L4: # x <= y  
    movq %rsi, %rax  
    subq %rdi, %rax  
    ret
```

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    long result;  
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    else  
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    return result;  
}
```

x in %rdi,
y in %rsi,
result in %rax

```
long switch_eg(long x, long y, long z) {  
    long w = 1;  
    switch(x) {  
    case 1:  
        w = y * z;  
        break;  
    case 2:  
        w = y / z; /* Fall Through */  
    case 3:  
        w += z;  
        break;  
    case 5:  
    case 6:  
        w -= z;  
        break;  
    default:  
        w = 2;  
    }  
    return w;  
}
```

```
absdiff:  
    cmpq %rsi, %rdi  
    # set flags for x-y  
    jle .L4  
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x in %rdi,
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result in %rax

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    }  
    return w;  
}
```

x in %rdi,
y in %rsi,
z in %rdx,
result in %rax

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    movq %rdi, %rax  
    subq %rsi, %rax  
    ret  
.L4: # x <= y  
    movq %rsi, %rax  
    subq %rdi, %rax  
    ret
```

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    case 6:  
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        break;  
    default:  
        w = 2;  
    }  
    return w;  
}
```

x in %rdi,
y in %rsi,
z in %rdx,
result in %rax

```
switch_eg:  
    movq %rdx, %rcx  
    cmpq $6, %rdi # x:6  
    ja .L8 # Use default  
    jmp *.L4(,%rdi,8)  
# ... code for each case.  
.Li: # in in 3,5,7,8,9  
...
```

```
.section .rodata .align 8  
.L4:  
    .quad .L8 #x == 0  
    .quad .L3 #x == 1  
    .quad .L5 #x == 2  
    .quad .L9 #x == 3  
    .quad .L8 #x == 4  
    .quad .L7 #x == 5  
    .quad .L7 #x == 6
```

Loops

Loops

```
long pcount_while(unsigned long x) {  
    long result = 0;  
    while (x) {  
        result += x & 0x1;  
        x >>= 1;  
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```
long pcount_goto_jtm(unsigned long x) {  
    long result = 0;  
    goto test;  
loop:  
    result += x & 0x1;  
    x >>= 1;  
test:  
    if (x)  
        goto loop;  
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    return result;  
}
```

```
long pcount_goto_dw(unsigned long x) {  
    long result = 0;  
    if (!x)  
        goto done;  
loop:  
    result += x & 0x1;  
    x >>= 1;  
    if (x)  
        goto loop;  
done:  
    return result;  
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    if (x)  
        goto loop;  
done:  
    return result;  
}
```

```
pcount_goto_jtm:  
    movl    $0,    %eax  
    jmp     .L2  
.L3:  
    movq    %rdi, %rdx  
    andl    $1,    %edx  
    addq    %rdx, %rax  
    shrq    %rdi  
.L2:  
    testq   %rdi, %rdi  
    jne     .L3  
    rep ret
```

Loops

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loop:
    result += x & 0x1;
    x >>= 1;
    if (x)
        goto loop;
done:
    return result;
}
```

```
pcount_goto_dw:
    testq %rdi, %rdi
    je .L4
    movl $0, %eax
.L3:
    movq %rdi, %rdx
    andl $1, %edx
    addq %rdx, %rax
    shrq %rdi
    jne .L3
    rep ret
.L4:
    movl $0, %eax
    ret
```

an often abused instruction:
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long m12(long x)
{
    return x*12;
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- Does **not** set condition codes,
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```
long m12(long x)
{
    return x*12;
}
```

```
m12:
    leaq (%rdi,%rdi,2), %rax # t <- x+x*2
    salq $2, %rax # return t<<2
    ret
```

The stack

The stack

- `%rsp` is special. It points to a location in memory called *the stack*.

`%rsp` →

The stack

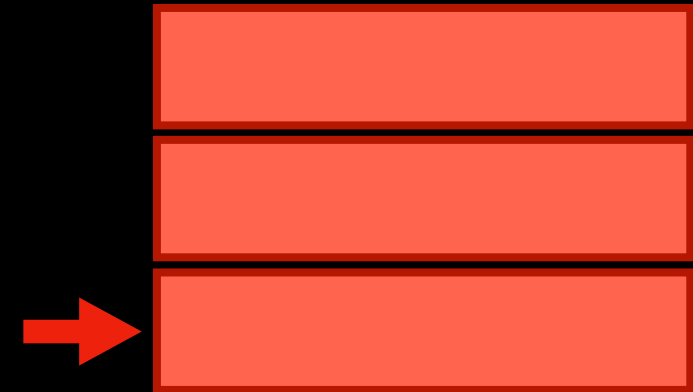
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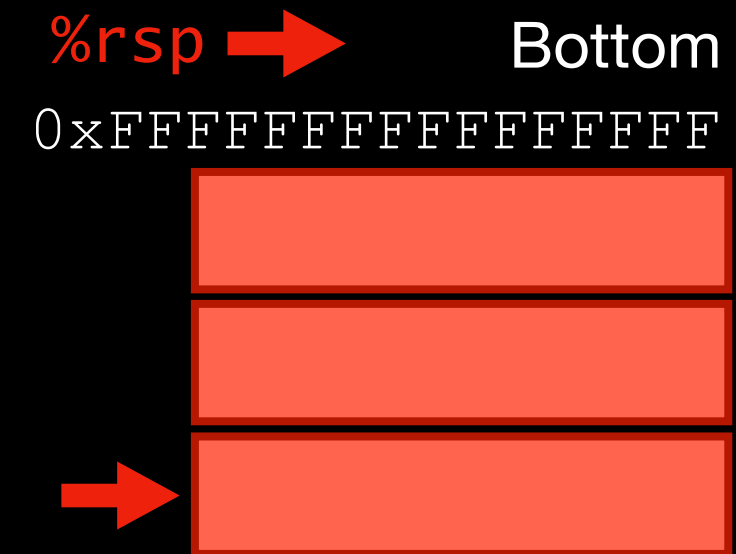
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...

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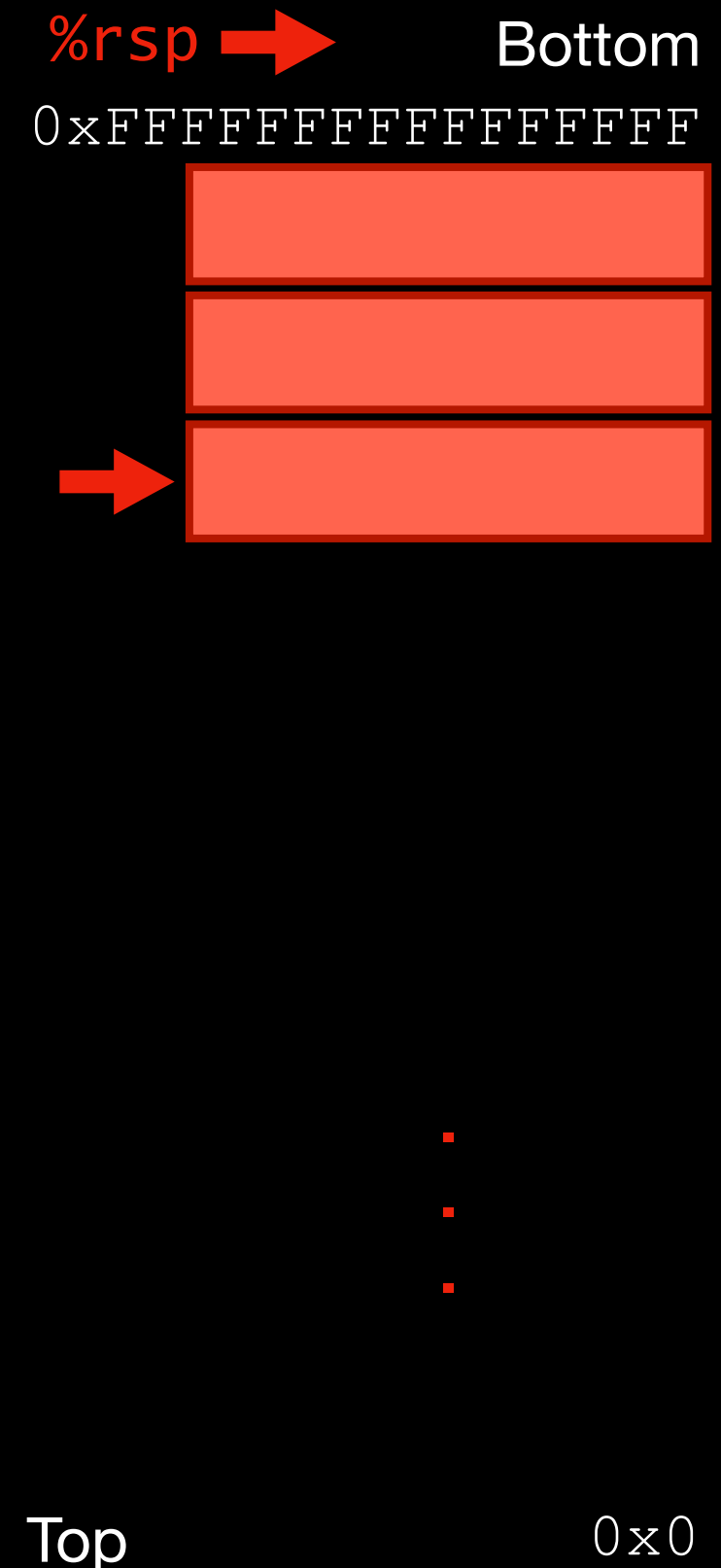


Top

0x0

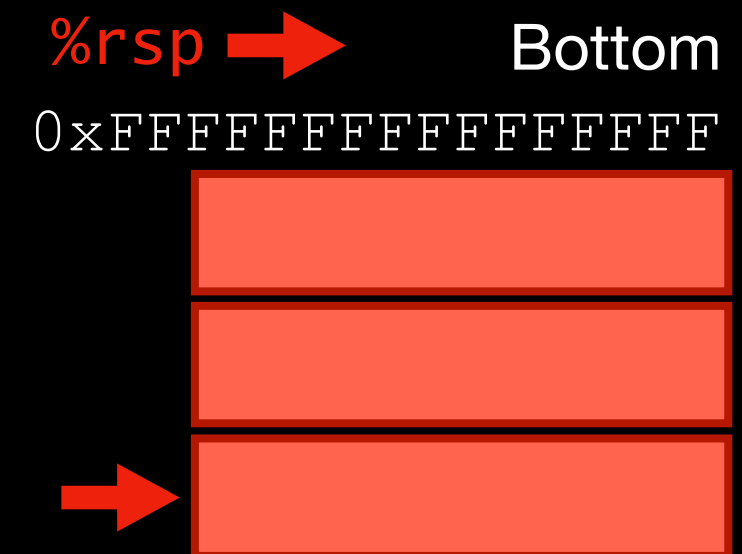
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 1. `%rsp -= 8`
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 2. write the `src` at `(%rsp)`
- `popq dest`
 1. read value from `(%rsp)` to `dest`
 2. `%rsp += 8`.



Top

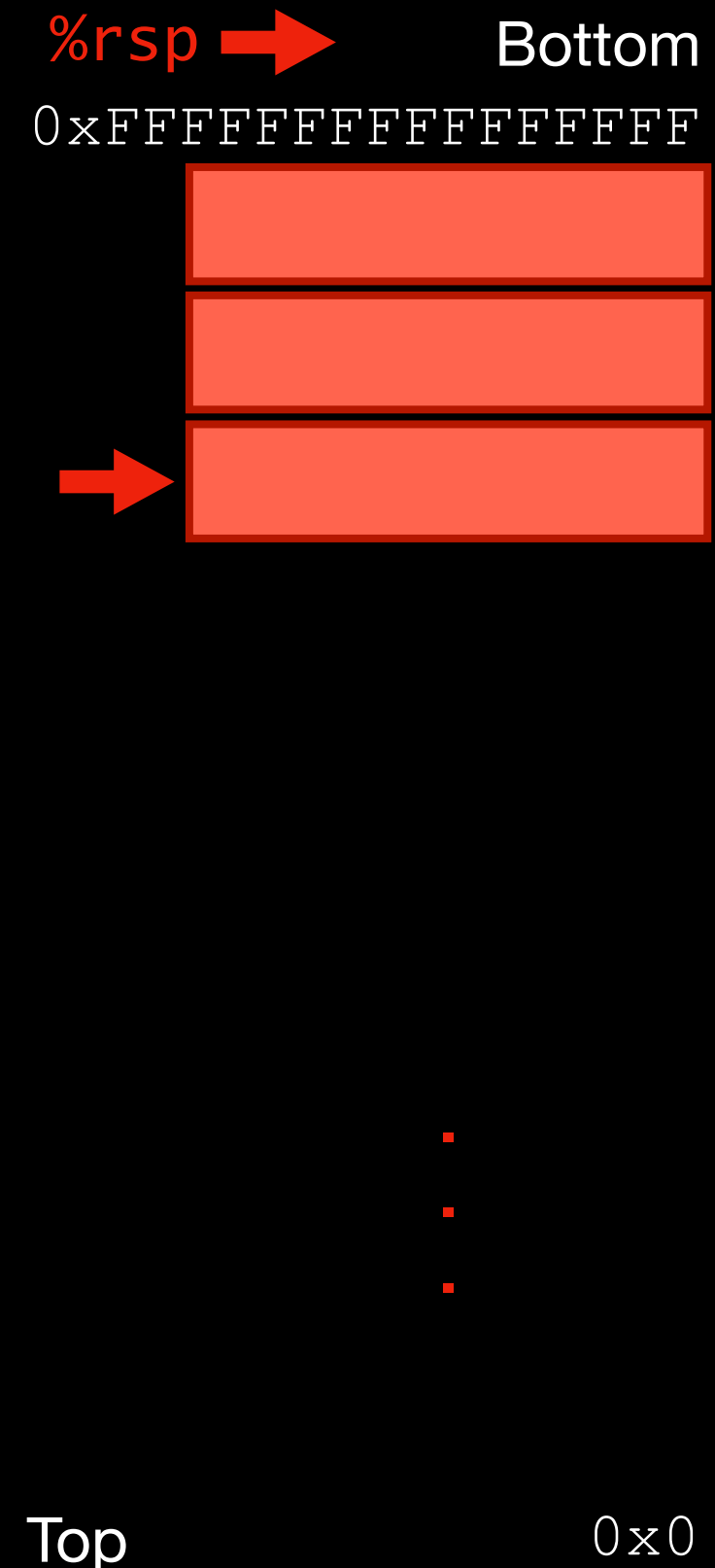
0x0

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- `popq dest`
 1. read value from `(%rsp)` to `dest`
 2. `%rsp += 8`.

`%rip`

```
example:
pushq $42
pushq $2020
pushq $3
popq %rdi
addq $8, %rsp
popq %rsi
```

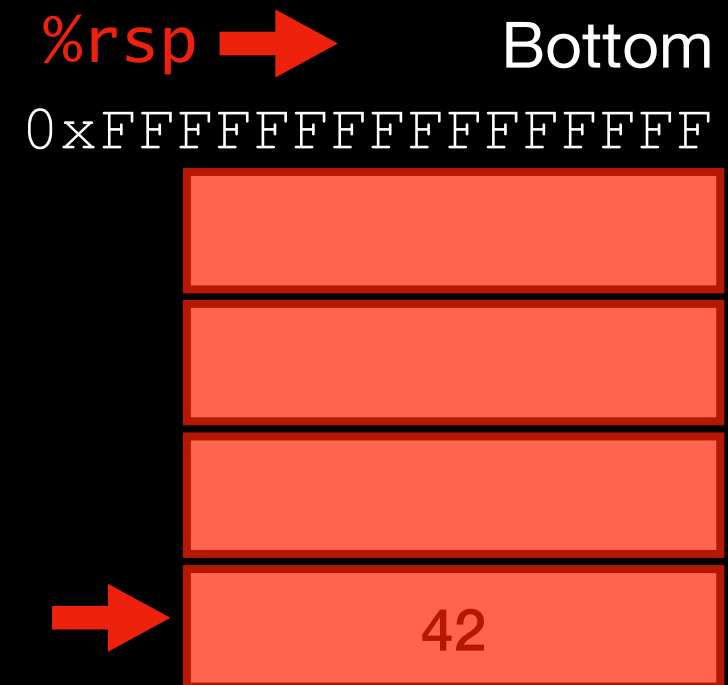


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popq %rsi
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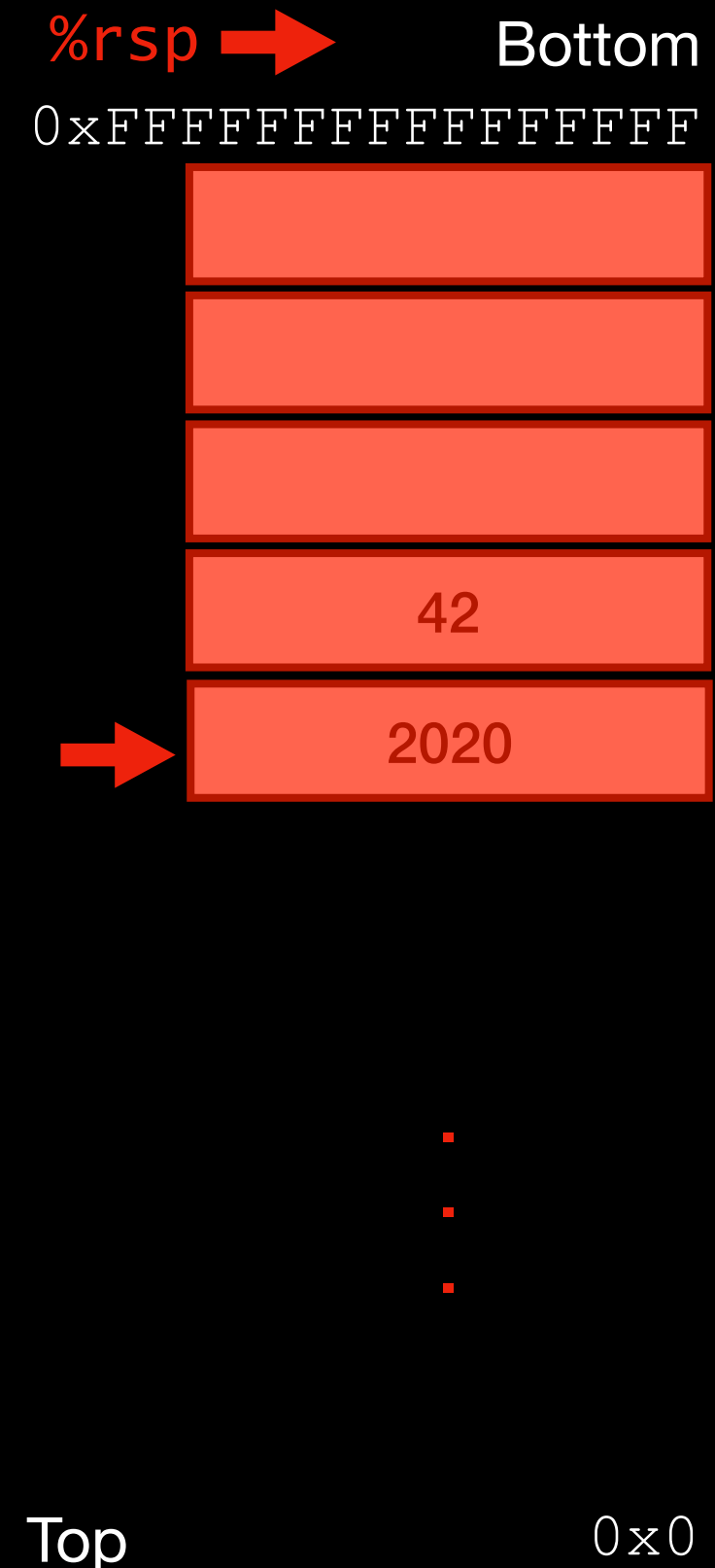


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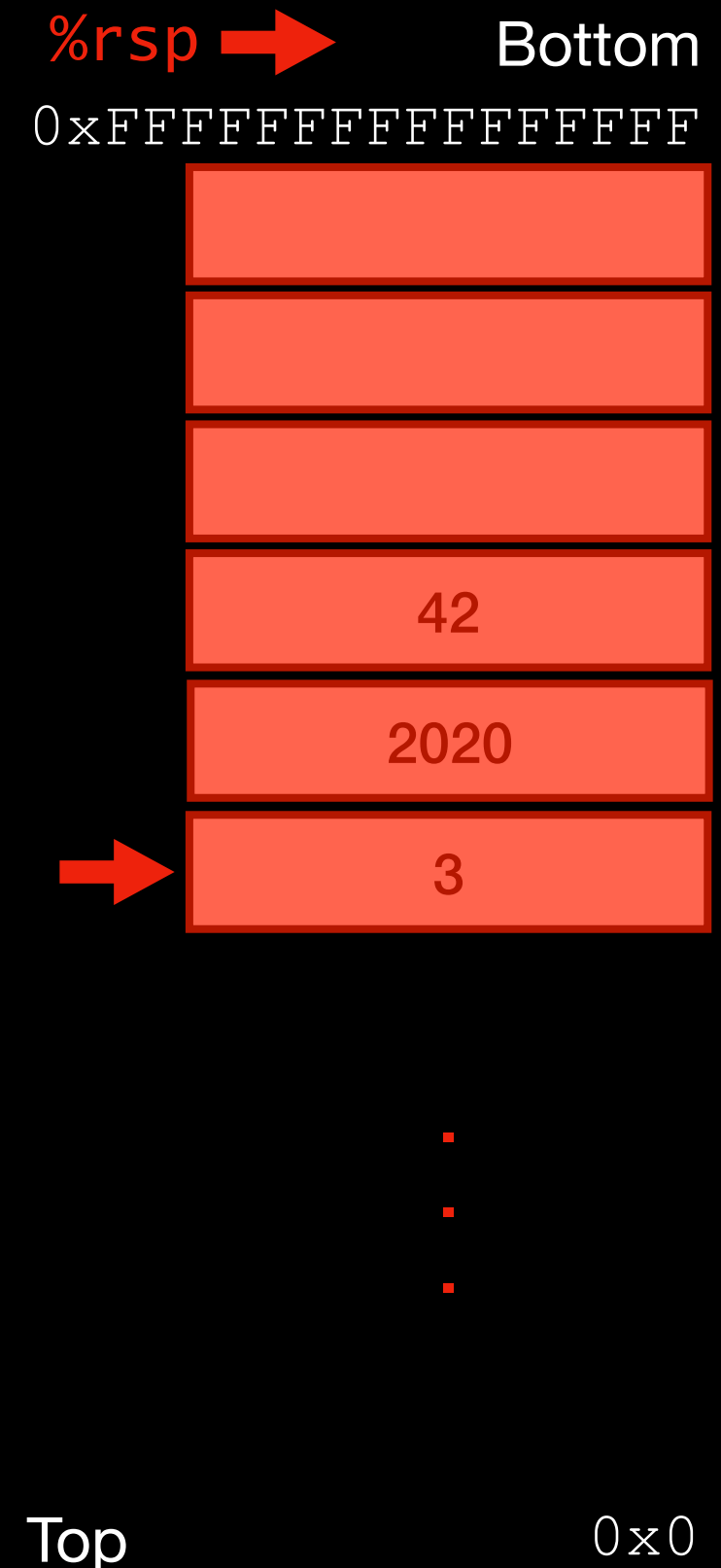


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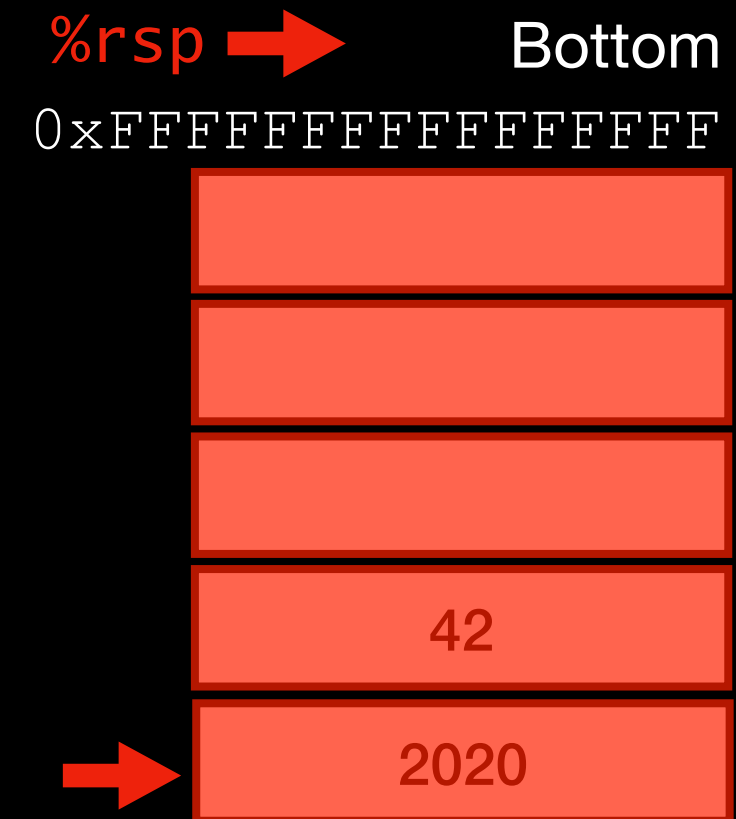


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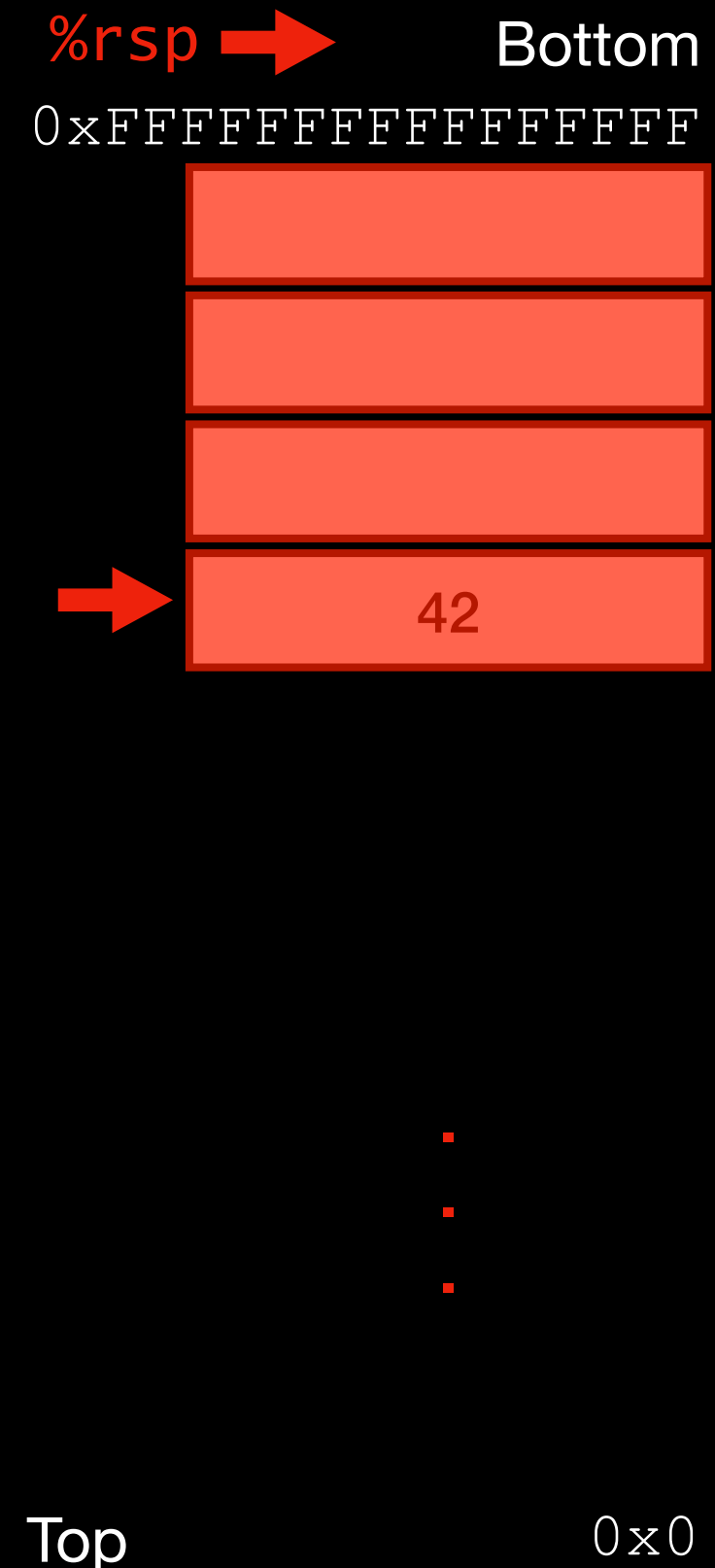
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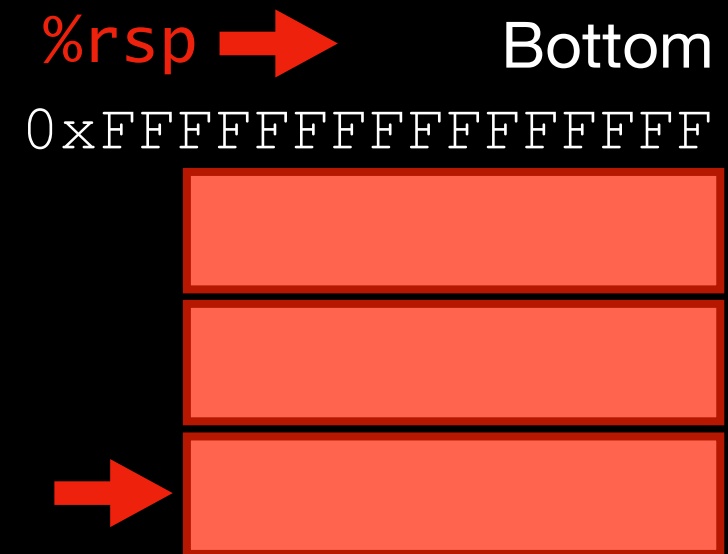
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0x0

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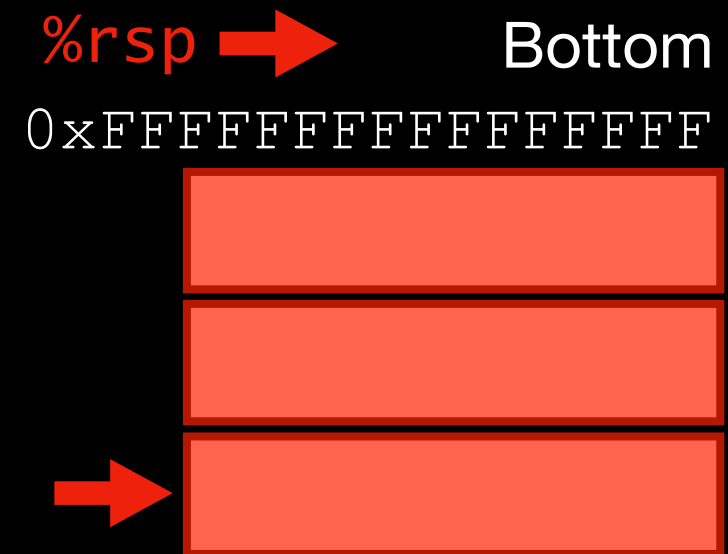
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 - drop a value with `addq $8, %rsp`,
 - make room for values using `subq`, and access them with `D(%rsp)`.

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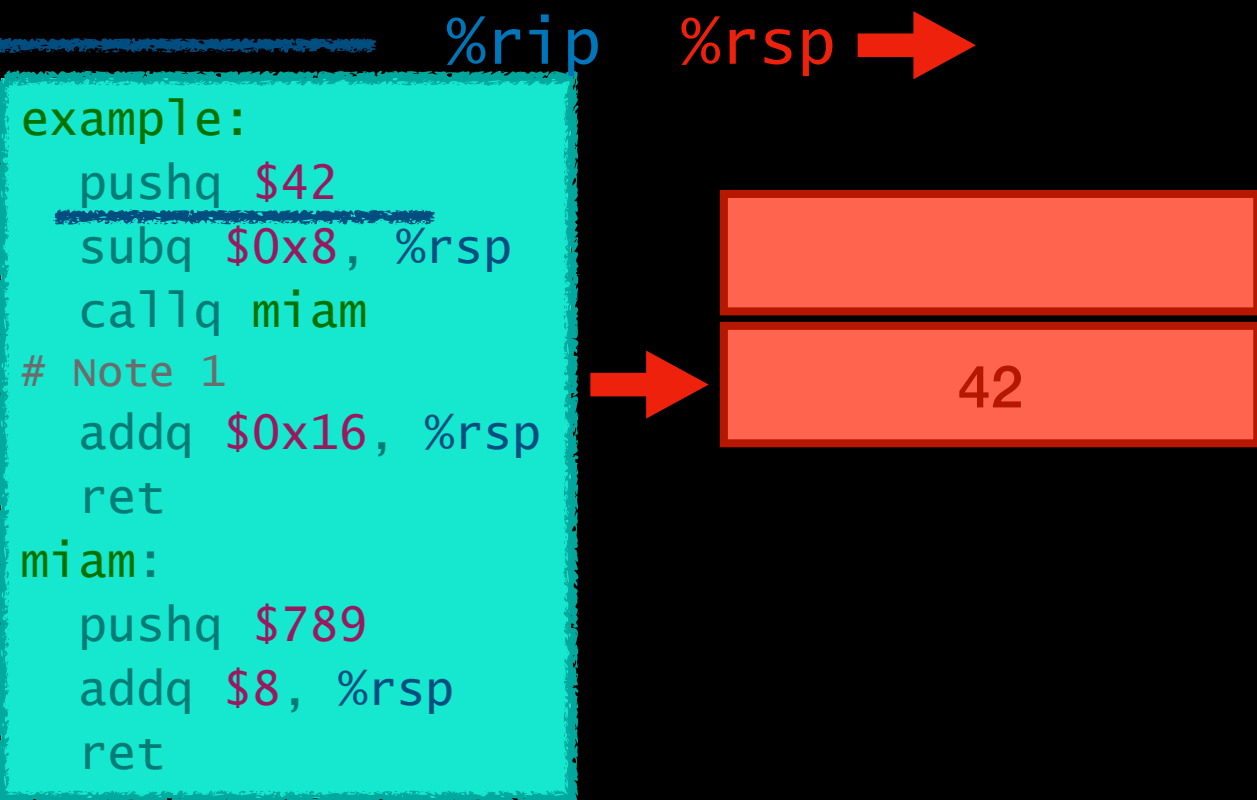
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example:
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    callq miam
# Note 1
    addq $0x16, %rsp
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miam:
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```

Note 1 : This comment is 11 (0xb) machine code bytes in example

Building functions

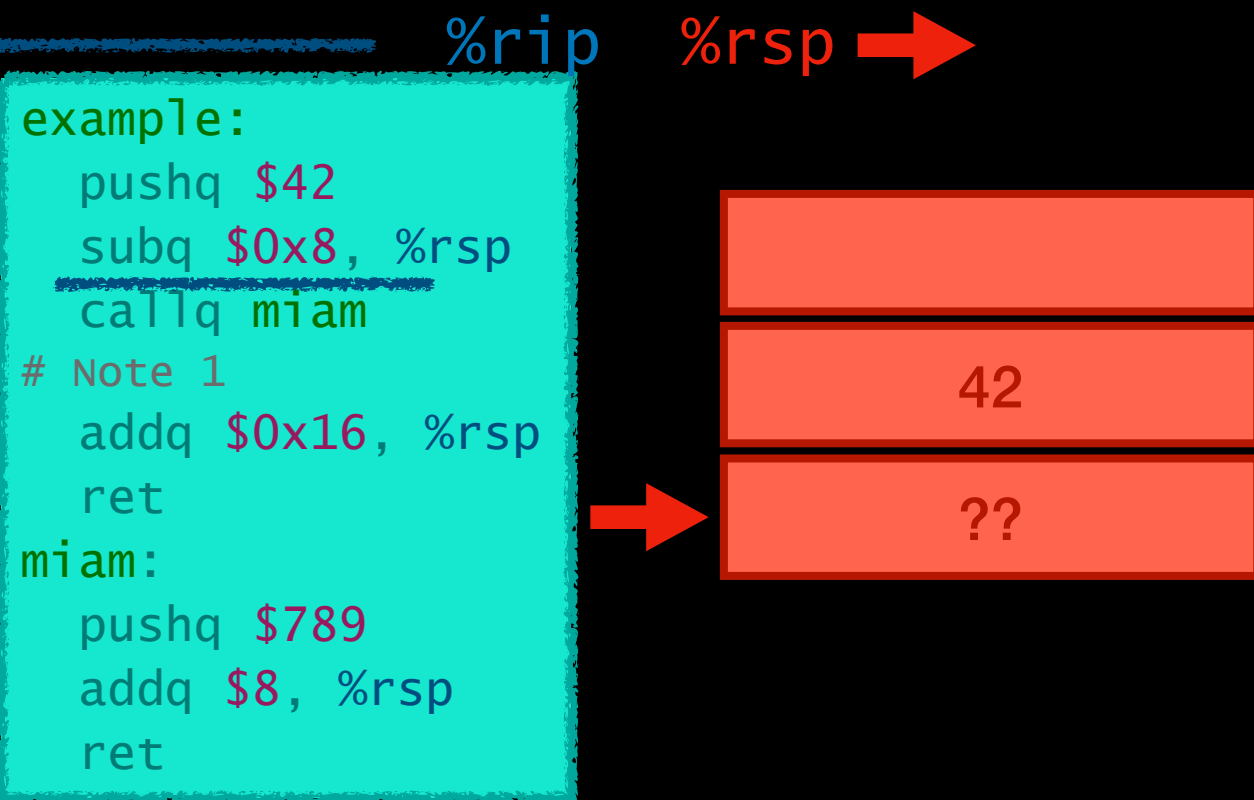
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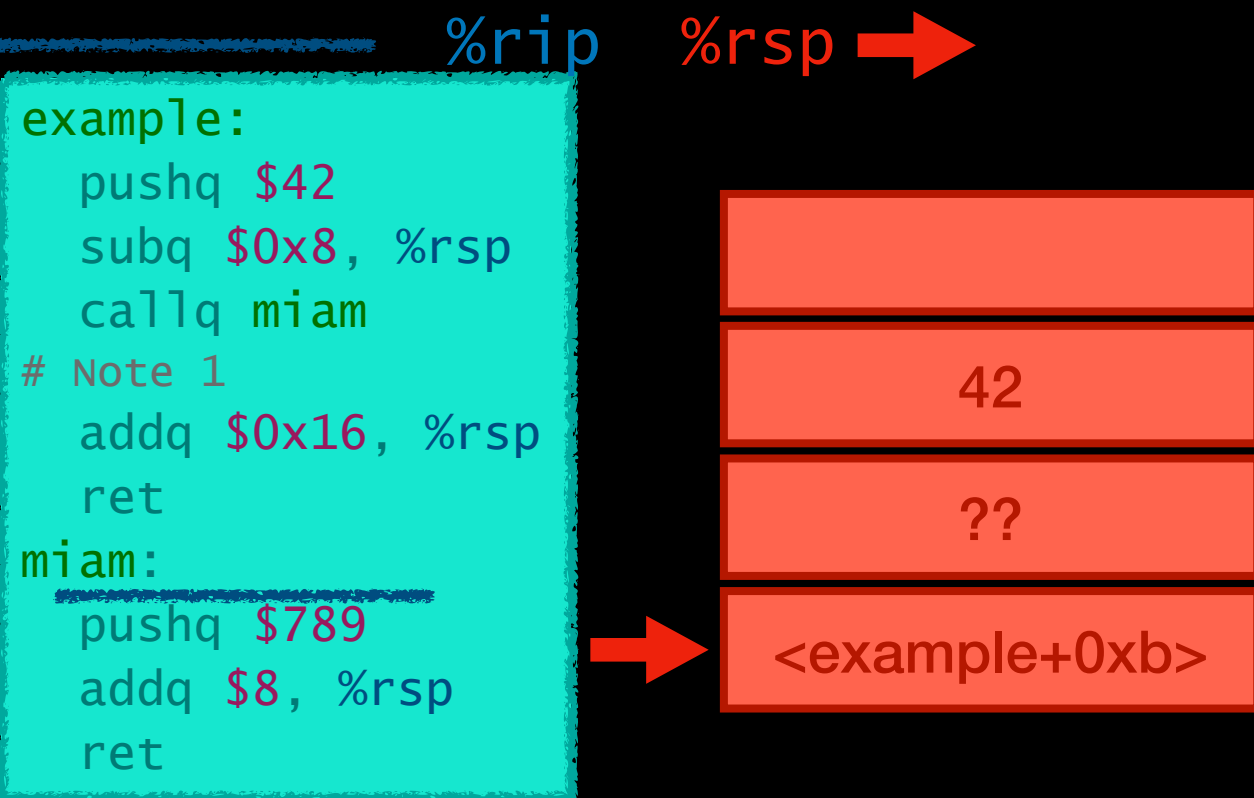
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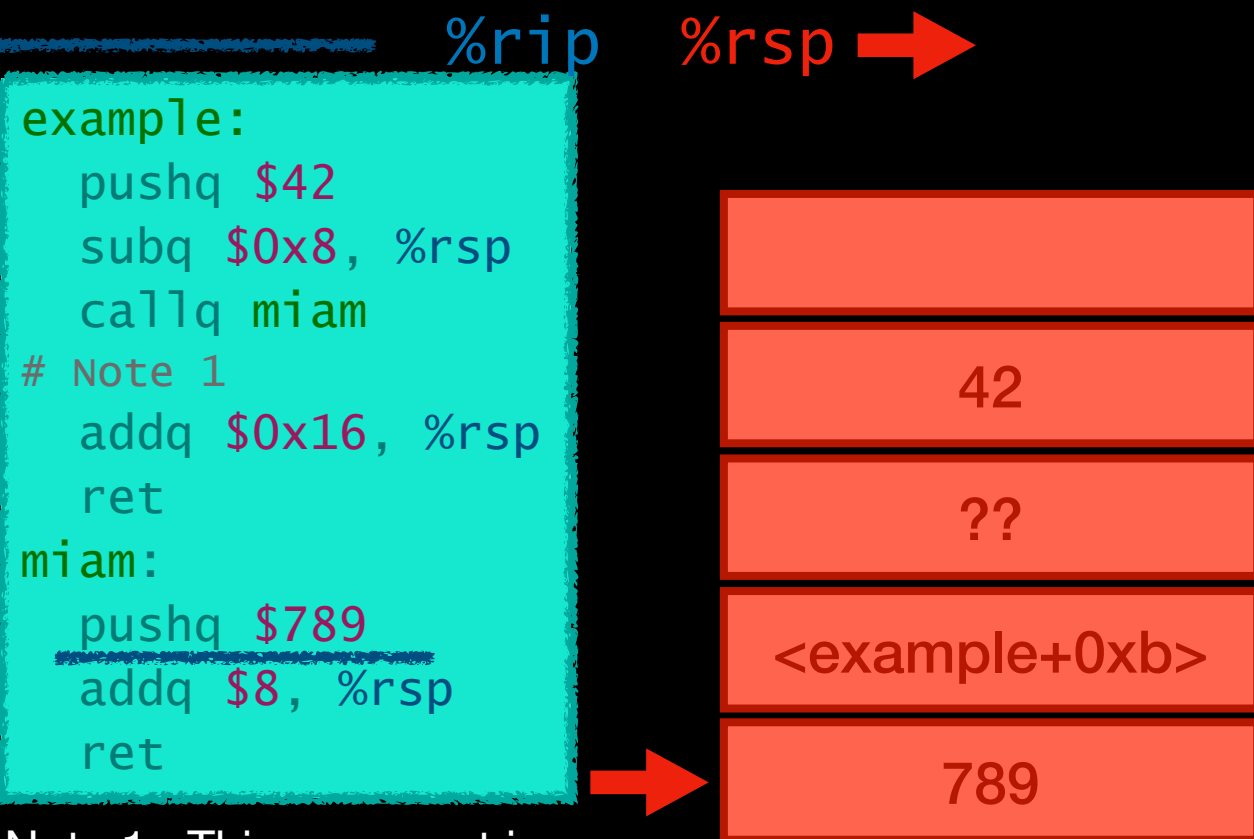
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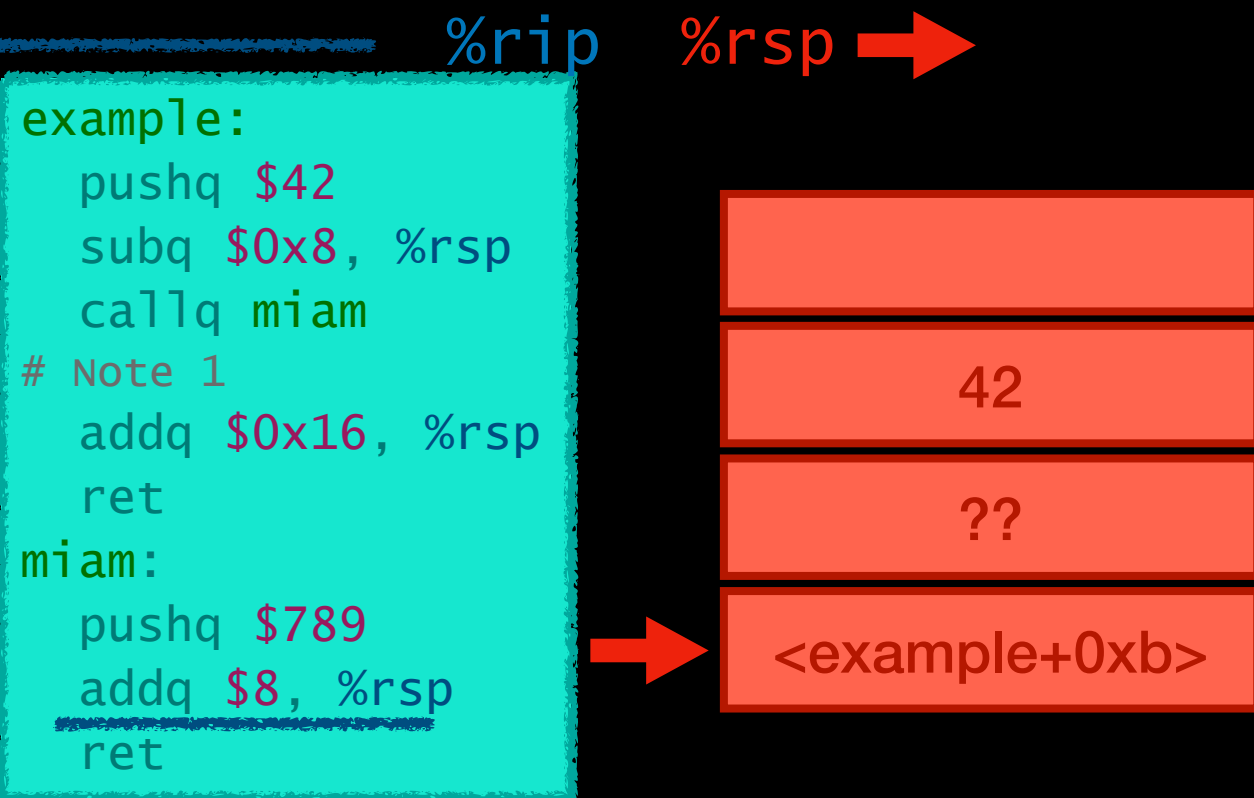
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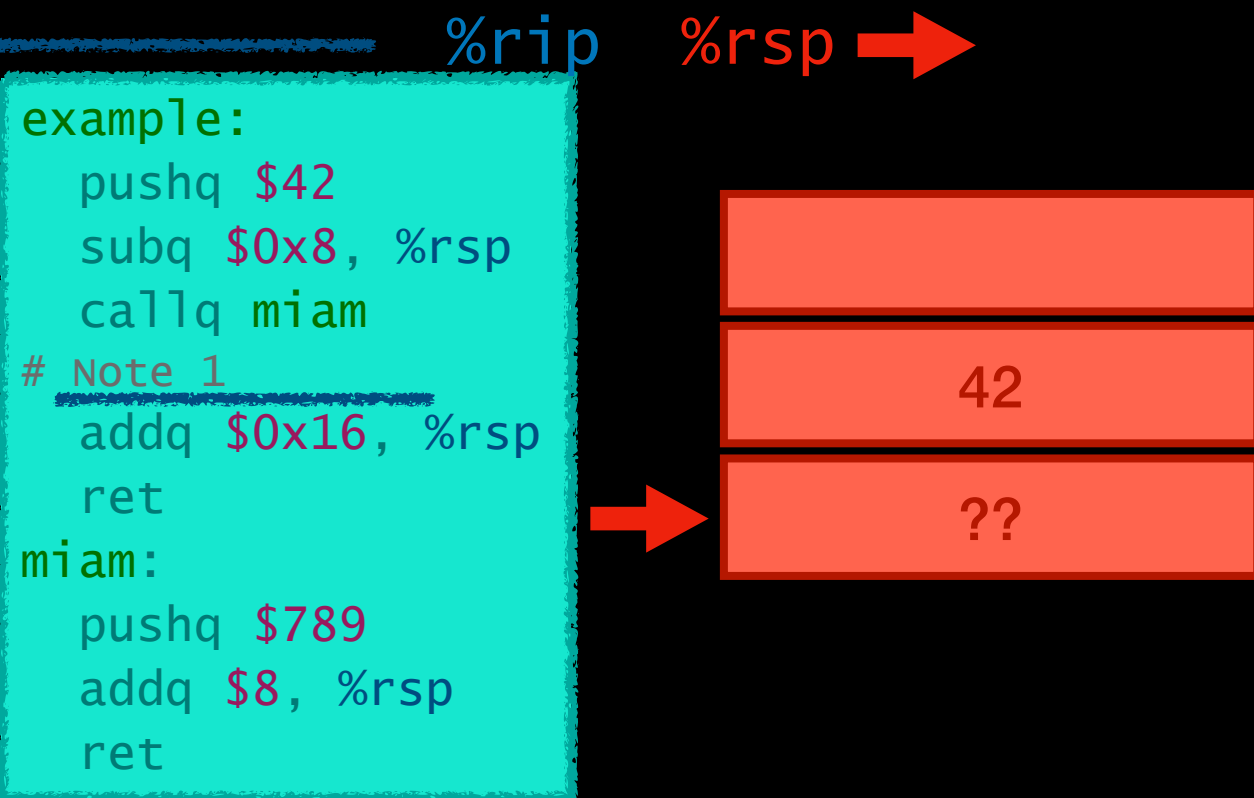
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- *Caller* saved register must be saved on the stack before calling functions if needed.
- *Callee* saved must be saved by the function that wants to use it.
- Too many arguments ? Use the stack !

%rax	%eax	%ax	%al	Return value	%r8	%r8d	%r8w	%r8b	5th arg
%rbx	%ebx	%bx	%bl	Callee saved	%r9	%r9d	%r9w	%r9b	6th arg
%rcx	%ecx	%cx	%cl	4th arg	%r10	%r10d	%r10w	%r10b	Caller saved
%rdx	%edx	%dx	%dl	3rd arg	%r11	%r11d	%r11w	%r11b	Caller saved
%rsi	%esi	%si	%sil	2nd arg	%r12	%r12d	%r12w	%r12b	Callee saved
%rdi	%edi	%di	%dil	1st arg	%r13	%r13d	%r13w	%r13b	Callee saved
%rbp	%ebp	%bp	%bpl	Callee saved	%r14	%r14d	%r14w	%r14b	Callee saved
%rsp	%esp	%sp	%spl	Stack ptr	%r15	%r15d	%r15w	%r15b	Callee saved

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long blah(long a, long b) {  
    return a * b - (a + b);  
}  
unsigned long fib(unsigned long n) {  
    if (n == 0) {  
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    } else if (n == 1) {  
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    }  
}  
  
int main() {  
    long a = blah(-42, -12) >> 2;  
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Which argument goes in which register ?

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main:  
    movq    $-42, %rdi  
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    callq   blah  
    shr     $2, %eax  
    and     $15, %eax  
    movq    %rax, %rdi  
    jmp     fib # TAILCALL
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```
fib:
    pushq   %r14
    pushq   %rbx
    movq    %rdi, %rbx
    testq   %rdi, %rdi
    je      LBB1_3
    cmpq    $1, %rbx
    jne     LBB1_5
    movl    $1, %ebx
LBB1_3:
    movq    %rbx, %rax
    jmp     LBB1_4
LBB1_5:
    leaq    -1(%rbx), %rdi
    callq   fib
    movq    %rax, %r14
    addq    $-2, %rbx
    movq    %rbx, %rdi
    callq   fib
    addq    %r14, %rax
LBB1_4:
    popq    %rbx
    popq    %r14
    retq
```

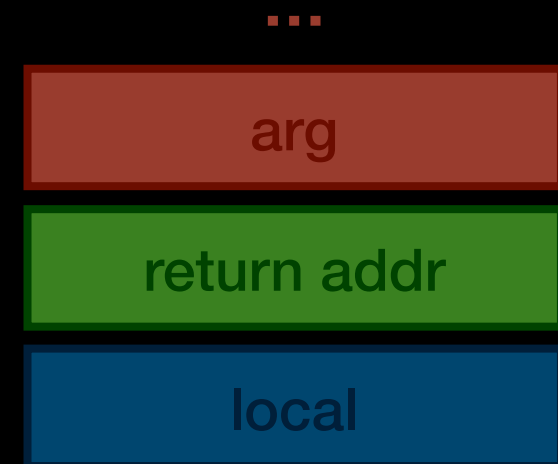
Stack frame

Stack frame

- Each function call takes up space on the stack

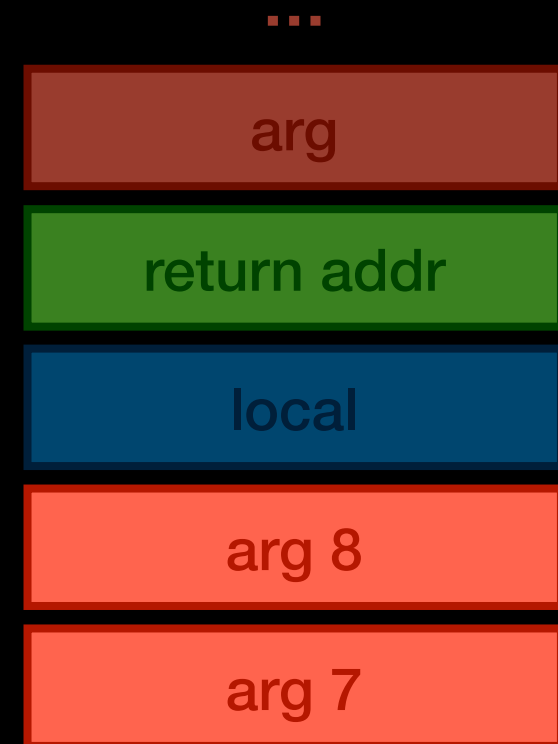
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Stack frame

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Stack frame

- Each function call takes up space on the stack
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 - Then the return address



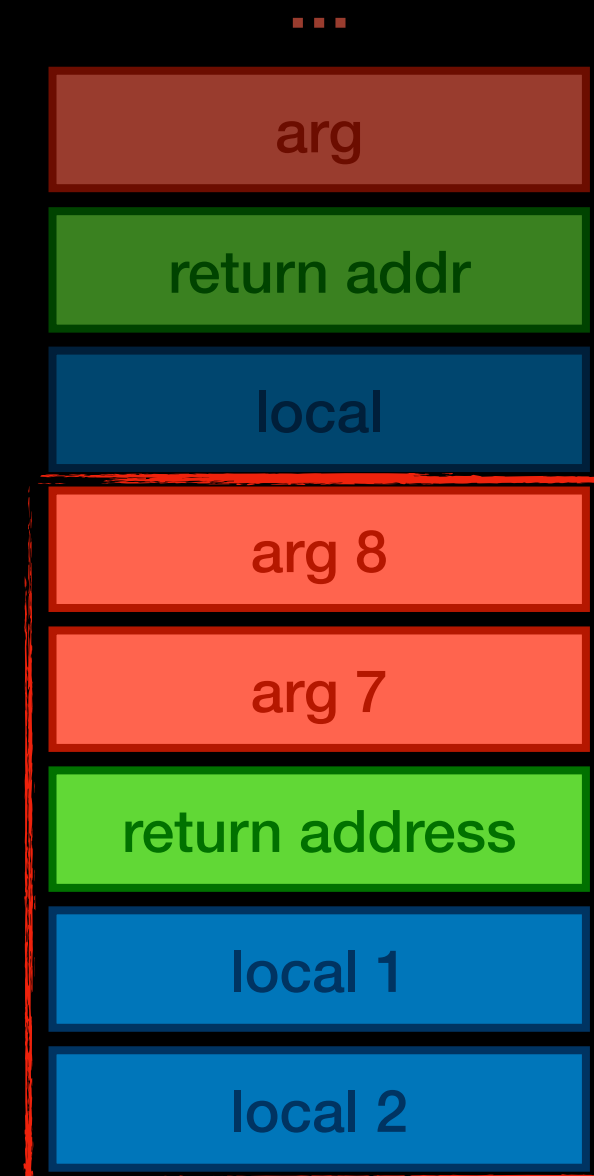
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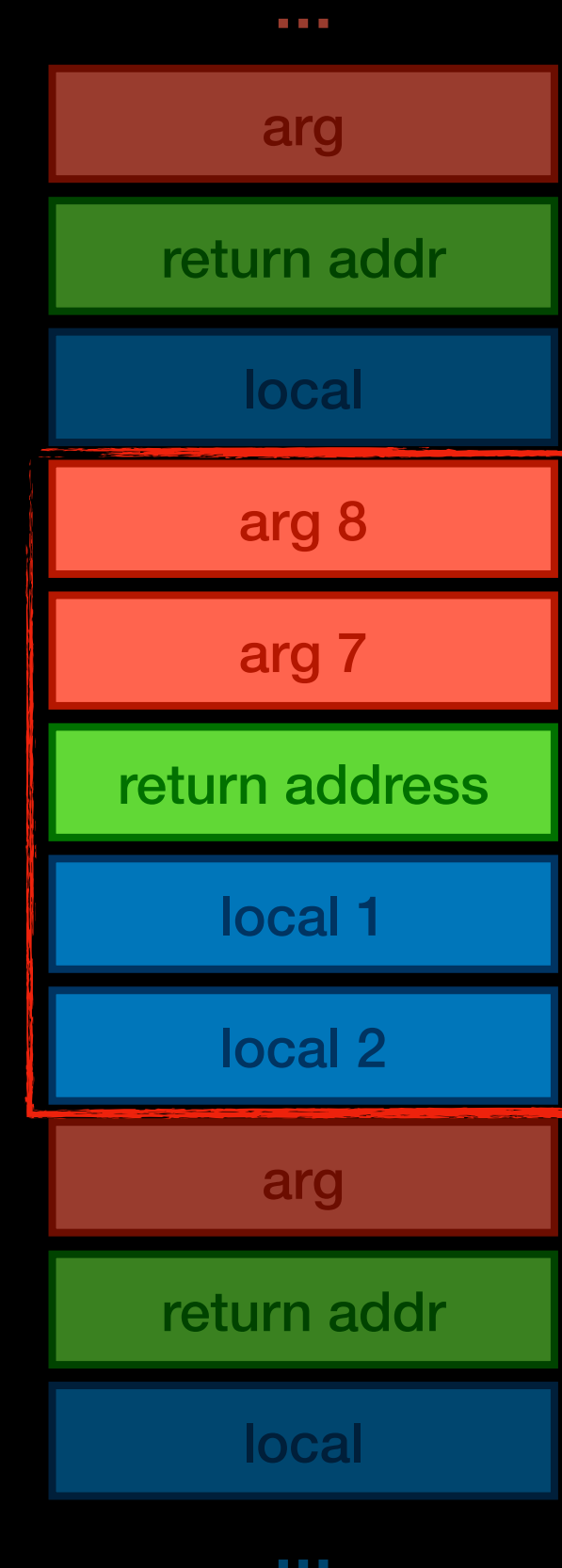
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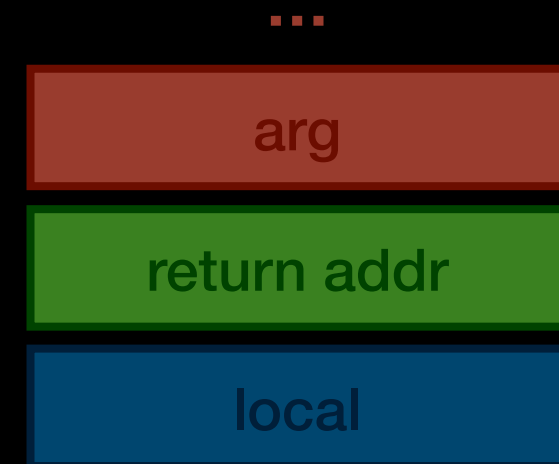
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 - First any arguments that had to be pushed on the stack
 - Then the return address
 - Then storage for local variable / spilling register
- We call all this the function's *stack frame*
- Each function call gets its own stack frame on the stack.
- Stack frame are freed up when function exit, in reverse order



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- Floating point, vector instructions
- Everything about privileges / OSs / performance / debugging.
- Microarchitecture (how CPU really work)

Closing words

This is not an exhaustive presentation, here's a list of things we haven't touched

- Mixing different register sizes (`movz/movs`)
- Some integer instructions
- Floating point, vector instructions
- Everything about privileges / OSs / performance / debugging.
- Microarchitecture (how CPU really work)
- See bibliography on the course website

Questions