Micro-Architectural Fault Attacks

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Fault attacks

- side channels: non-legitimate “read primitive”

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Fault attacks

- side channels: non-legitimate “read primitive”
- can we have a “write primitive”?
- yes! fault attacks!
- why is that a problem? hardware can bypass software security mechanisms
  $\rightarrow$ software cannot trust hardware anymore

Software-based fault attacks?

- until 2014, fault attacks required physical access: changes in temperature, clock, voltage, electric/magnetic fields, ...

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- first reaction: "it's a reliability issue, not a security issue"

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- first reaction: "it's a reliability issue, not a security issue"
- 2015: Google Project Zero showed a sandbox escape and a privilege escalation attack using Rowhammer

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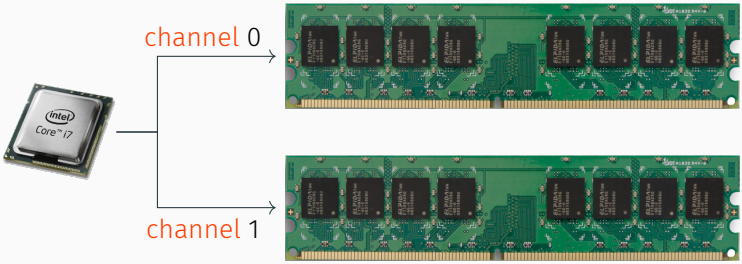
Outline

- Background on DRAM and Rowhammer
- How do we get bip flips?
- How do we target memory accesses?
- Can we exploit these bit flips?
- Countermeasures

Background on DRAM and Rowhammer

DRAM organization

DRAM organization



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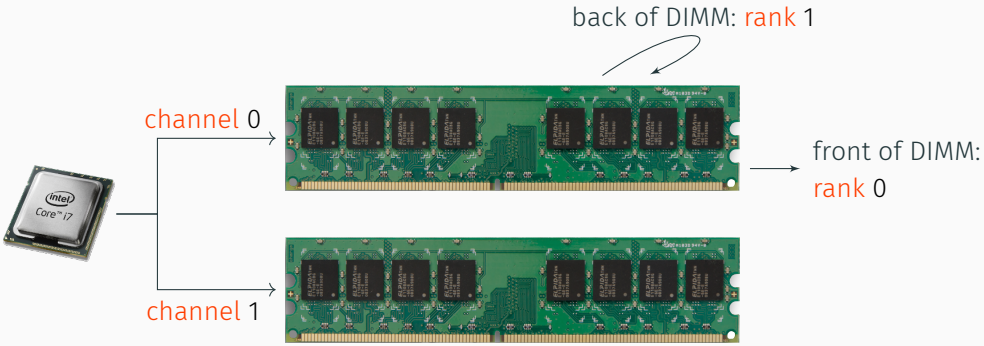

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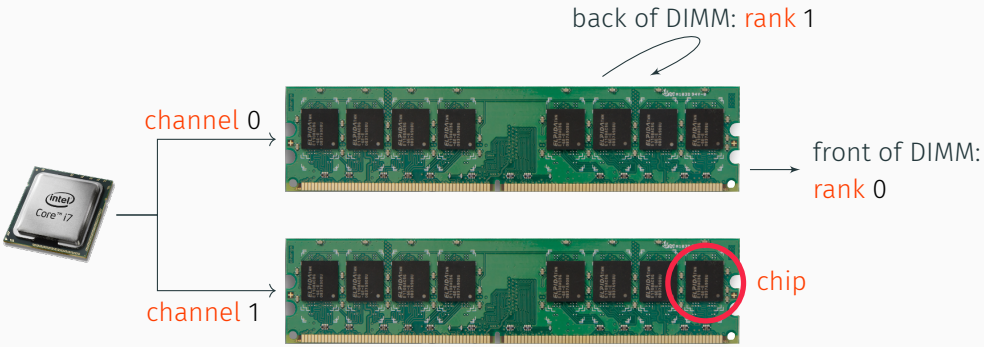

DRAM organization

chip

bank 0

row 0
row 1
row 2
...
row 32767

row buffer

DRAM organization

chip

bank 0

row 0
row 1
row 2
...
row 32767

row buffer

64k cells
1 capacitor,
1 transitor each

DRAM row buffer

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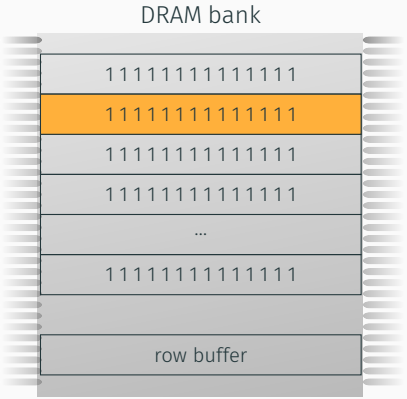
→ row buffer

How reading from DRAM works



CPU wants to access row 1

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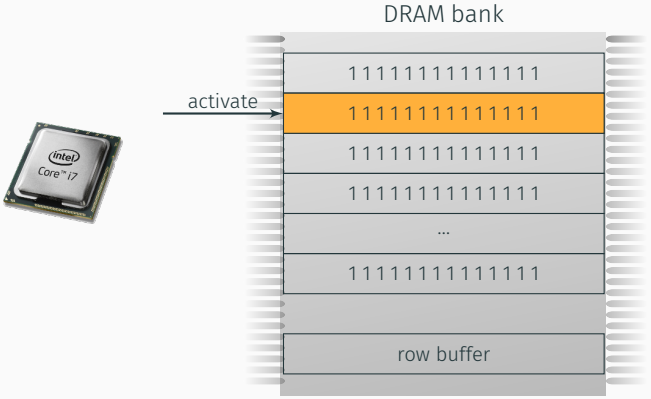

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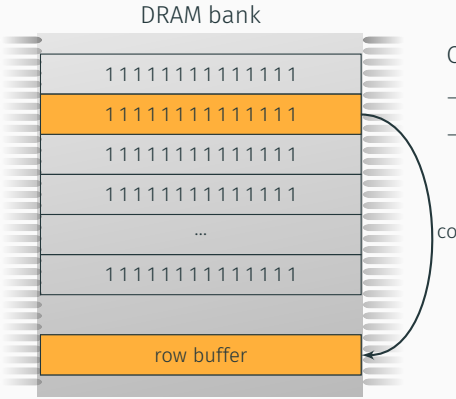

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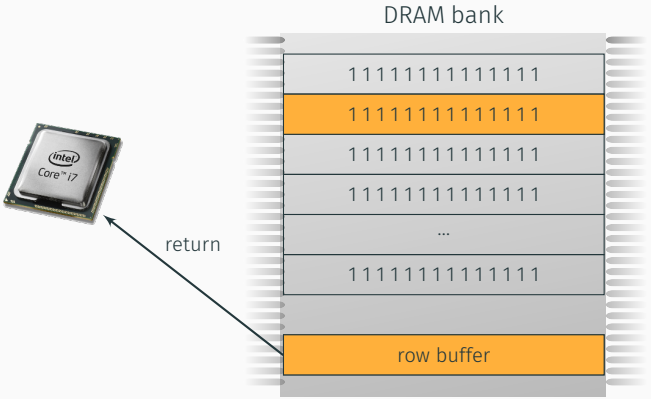

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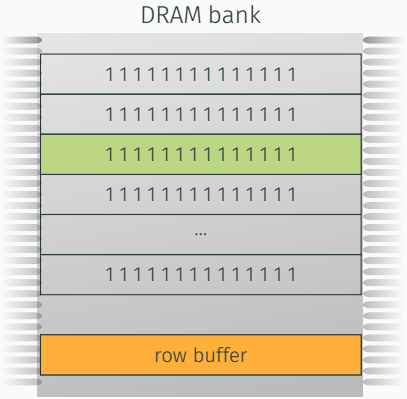
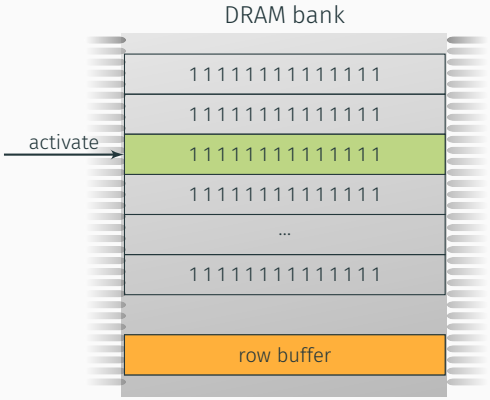


CPU wants to access row 2

How reading from DRAM works



CPU wants to access row 2

$\rightarrow$ row 2 activated

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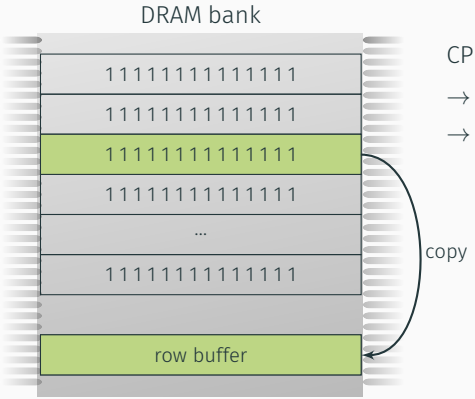

CPU wants to access row 2

→ row 2 activated

→ row 2 copied to row buffer

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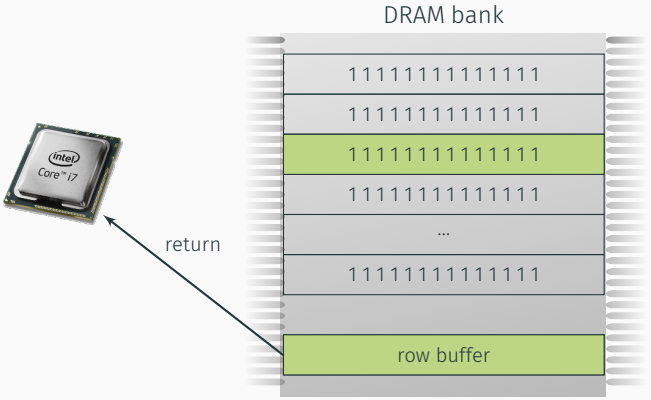

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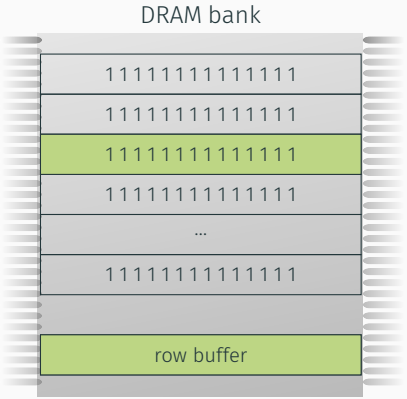


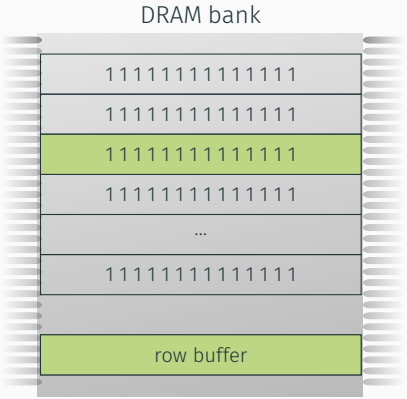
CPU wants to access row 2

→ row 2 activated

→ row 2 copied to row buffer

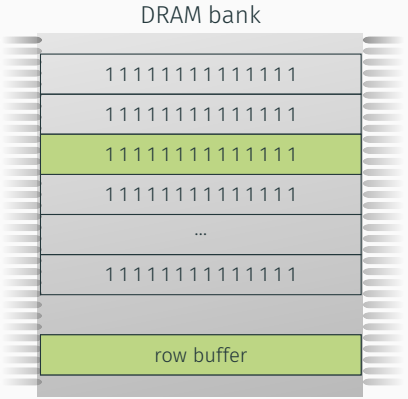
→ slow (row conflict)

How reading from DRAM works



CPU wants to access row 2—again

How reading from DRAM works



CPU wants to access row 2—again

→ row 2 already in row buffer

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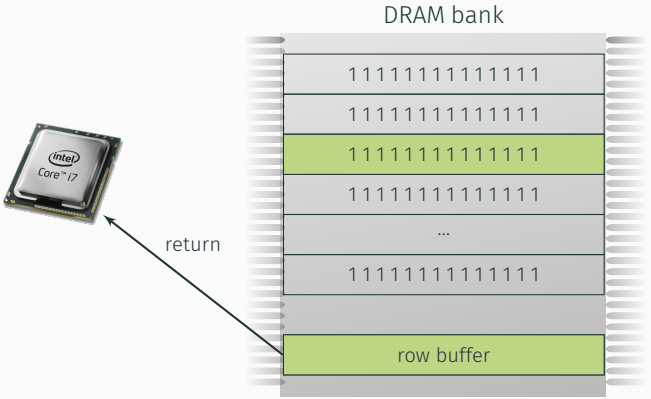

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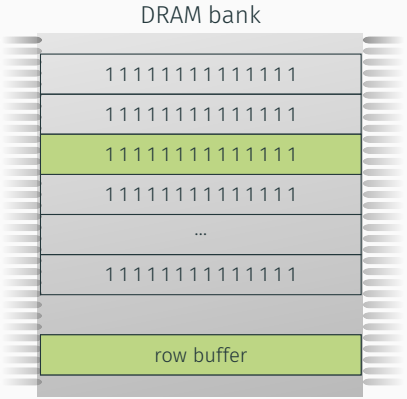

CPU wants to access row 2—again

→ row 2 already in row buffer

→ fast (row hit)

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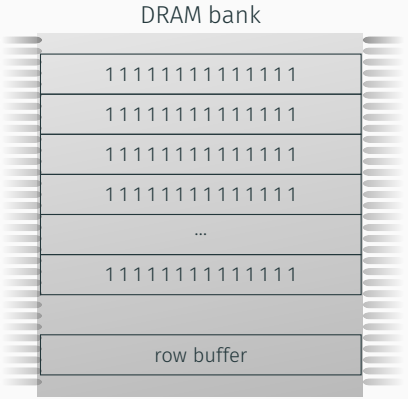

row buffer = cache

DRAM refresh

- cells leak $\rightarrow$ repetitive refresh necessary
- refresh $\approx$ reading (destructive) + writing same data again
- maximum interval between refreshes to guarantee data integrity

DRAM refresh

- cells leak → repetitive refresh necessary
- refresh ≈ reading (destructive) + writing same data again
- maximum interval between refreshes to guarantee data integrity

- cells leak faster upon proximate accesses → fault attack

Rowhammer

"It's like breaking into an apartment by repeatedly slamming a neighbor's door until the vibrations open the door you were after" – Motherboard Vice

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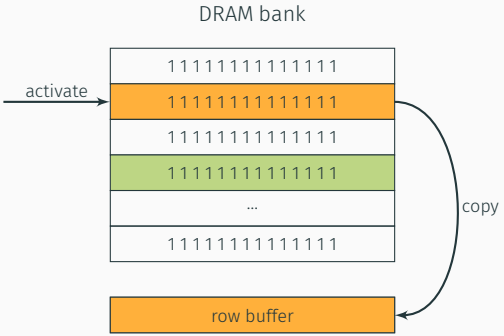

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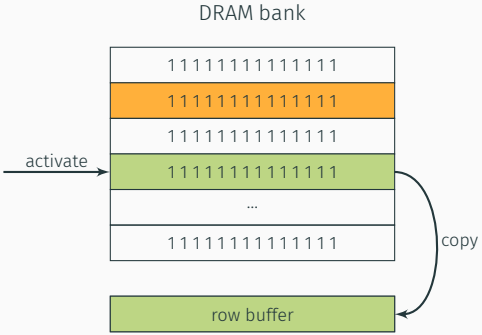

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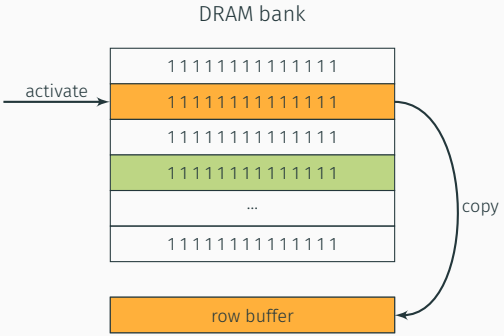

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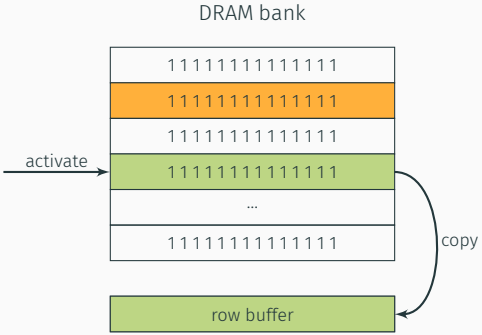

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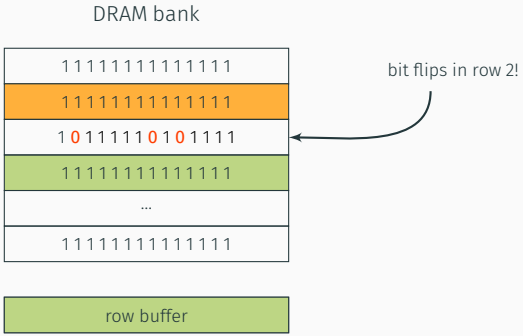


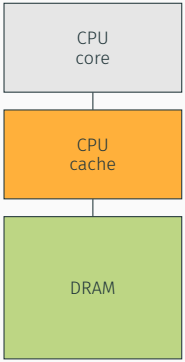
Requirements

Memory accesses must be

- uncached: reach DRAM
- fast: race against the next row refresh
- targeted: reach specific row

Issue #1: How do we get bit flips?

Impact of the CPU cache



- only non-cached accesses reach DRAM
- original attacks use `clflush` instruction

→ flush line from cache

→ next access will be served from DRAM

How to reach DRAM?

1. `clflush` instruction → original paper (Kim et al.)
2. cache eviction (Gruss et al., Aweke et al.)
3. non-temporal accesses (Qiao et al.)
4. uncached memory (van der Veen et al.)
5. remotely (Lipp et al., Tatar et al.)

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Rui Qiao et al. “A new approach for rowhammer attacks”. In: *HOST 2016*. 2016.

Victor van der Veen et al. “Drammer: Deterministic Rowhammer Attacks on Mobile Platforms”. In: *CCS’16*. 2016.

Moritz Lipp et al. “Nethammer: Inducing Rowhammer Faults through Network Requests”. In: *arXiv:1805.04956* (2018).

Andrei Tatar et al. “Throwhammer: Rowhammer Attacks over the Network and Defenses”. In: *USENIX ATC 2018*. 2018.

#1 Hammering with `clflush`

```
begin:
  mov (X), %eax   // read from address X
  mov (Y), %ebc   // read from address Y
  clflush (X)     // flush cache for address X
  clflush (Y)     // flush cache for address Y
  jmp begin
```

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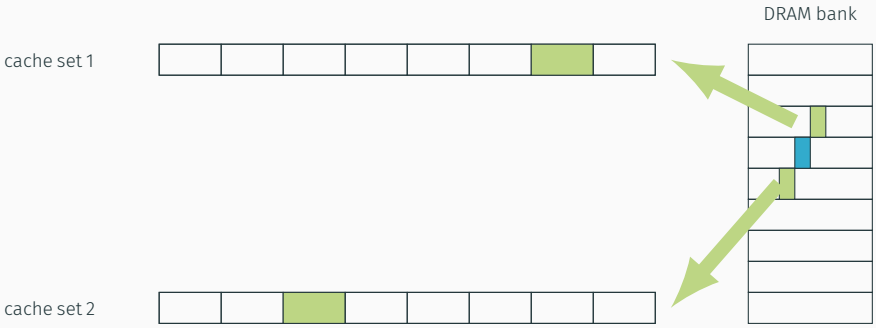

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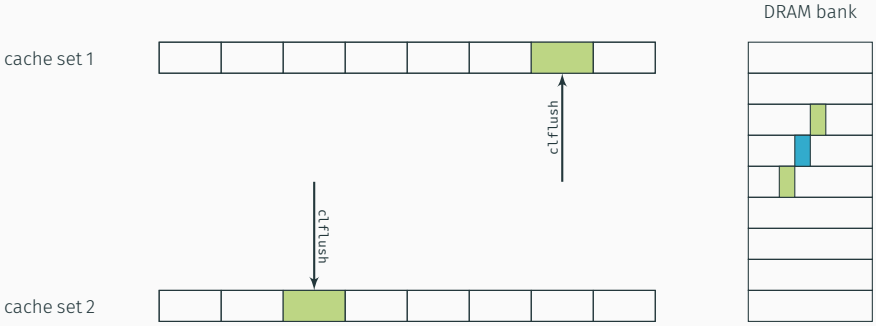

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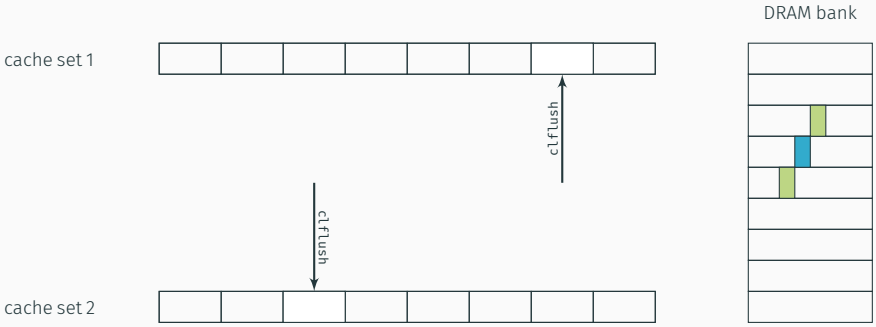

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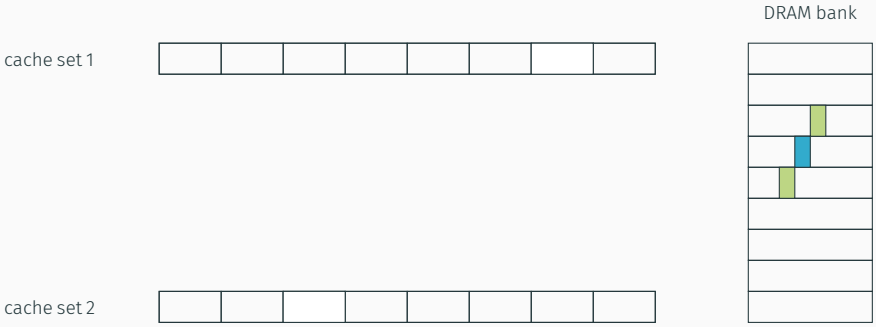

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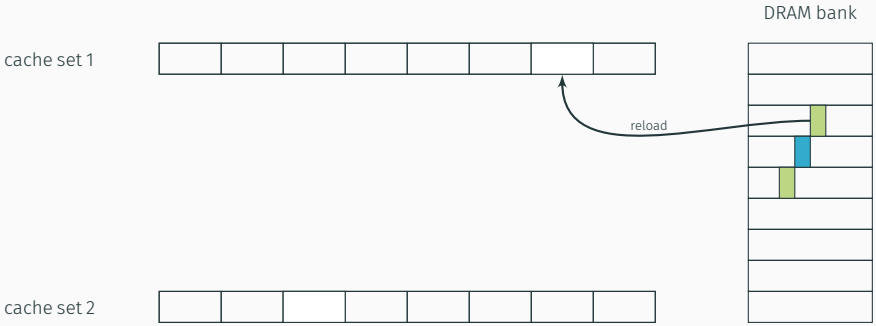

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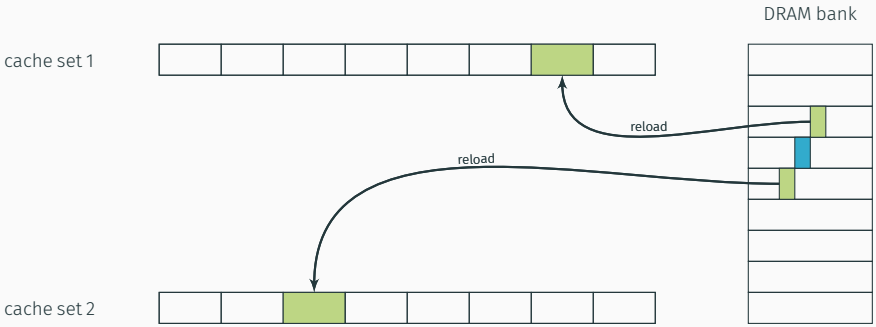

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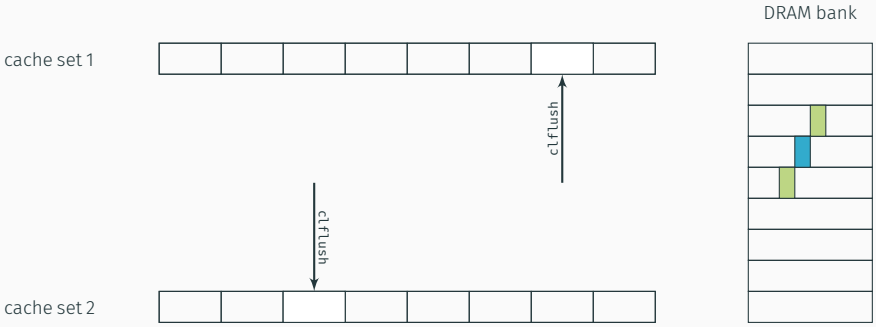

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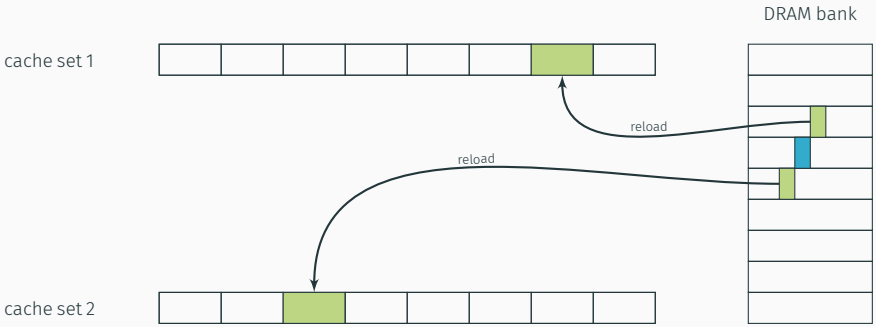

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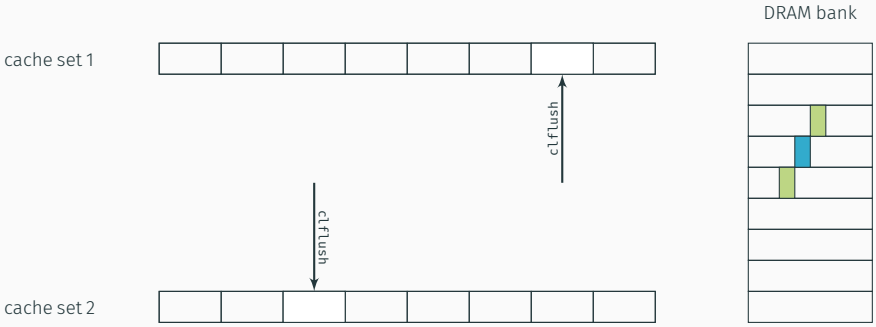

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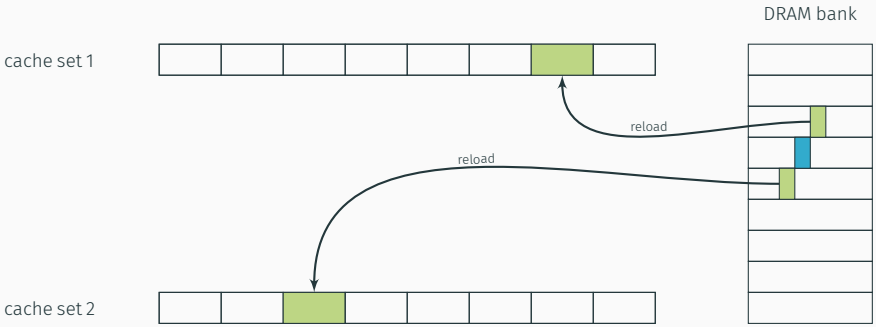

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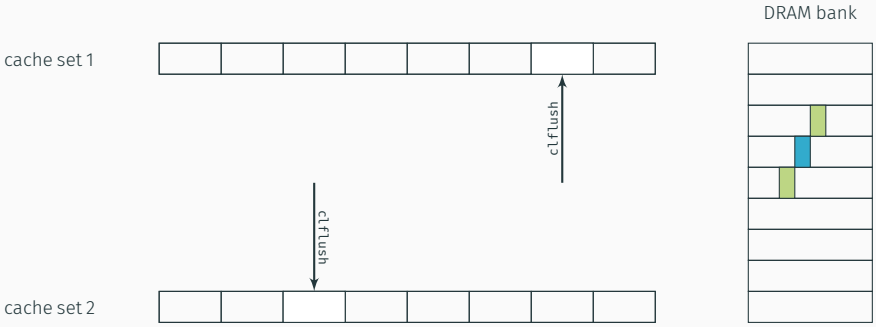

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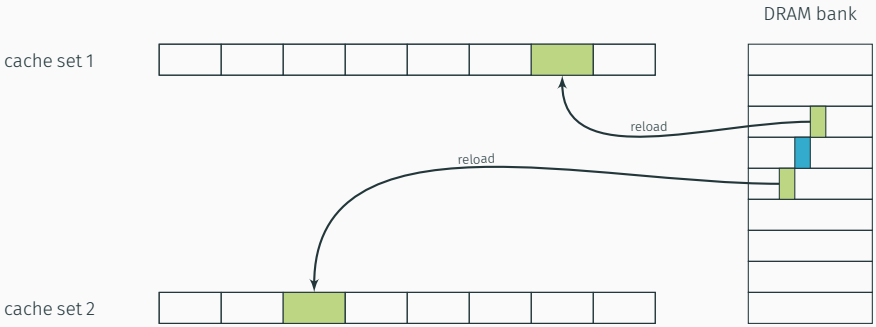

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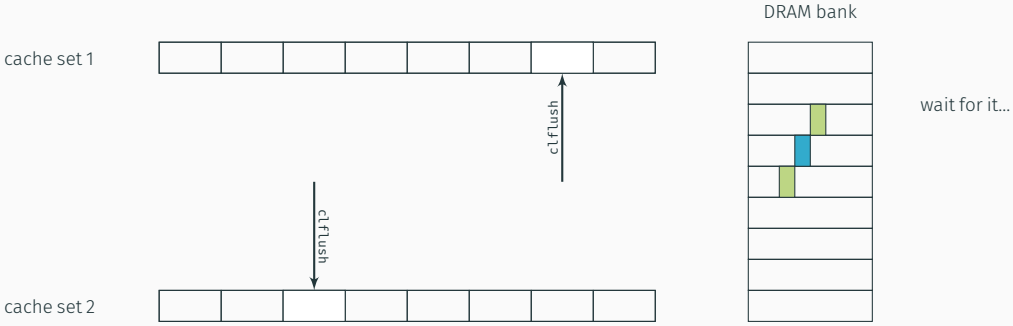

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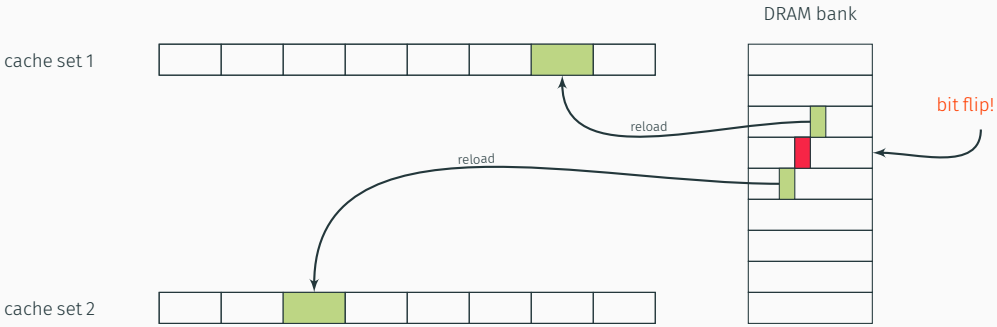

Flush, reload, flush, reload...

- the core of Rowhammer is essentially a Flush+Reload loop
- as much an attack on DRAM as on cache

#2 Hammering with cache eviction

- idea: avoid `clflush` to be independent of specific instructions
  → no `clflush` in JavaScript

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- beware of the replacement policy!

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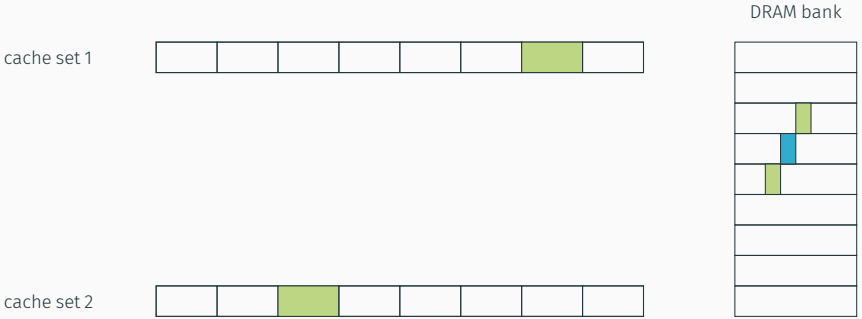

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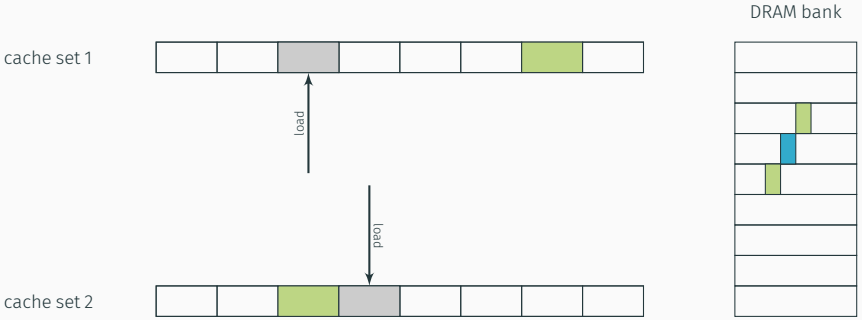

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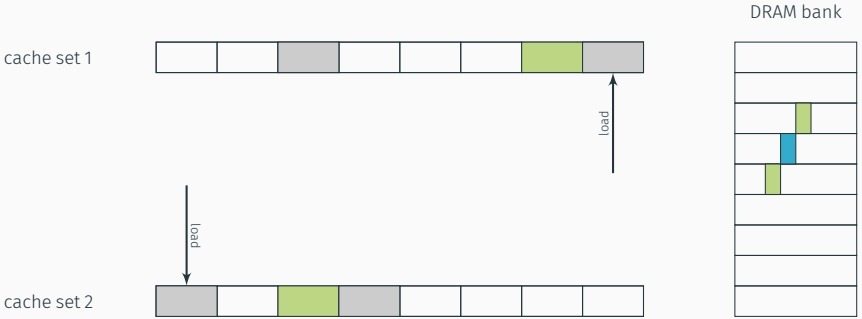

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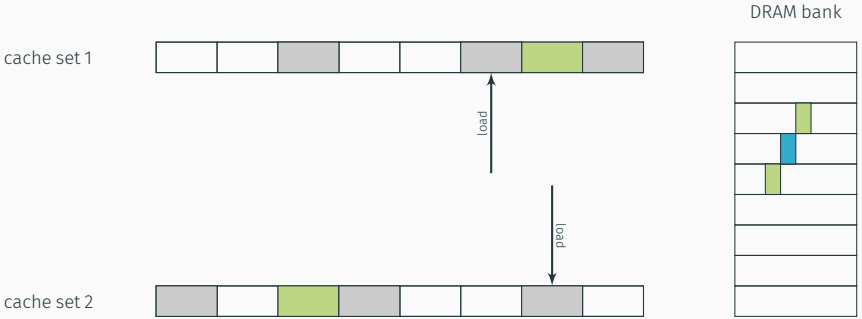

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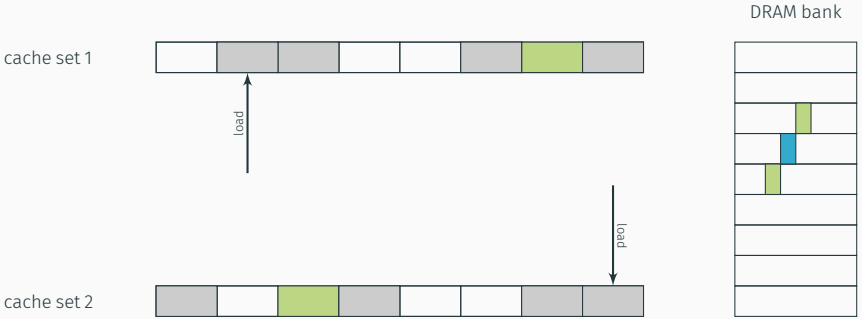

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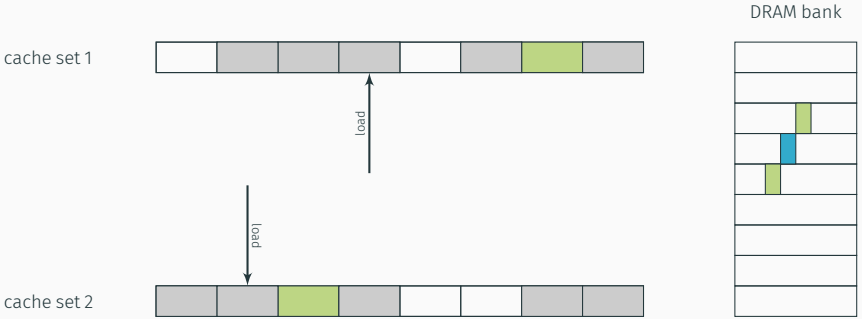

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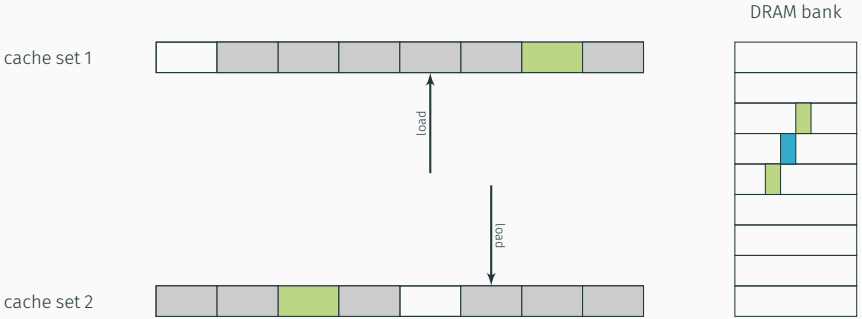

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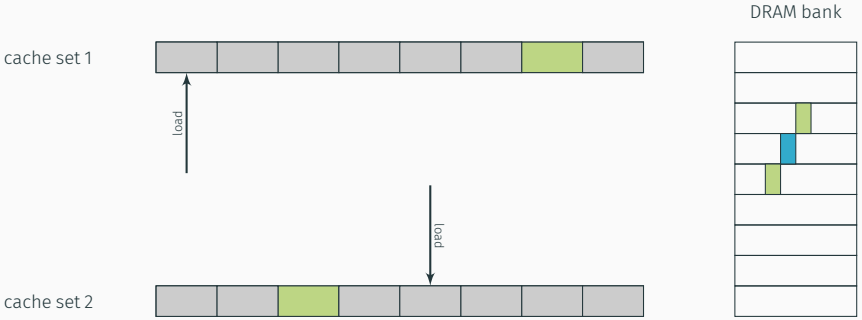

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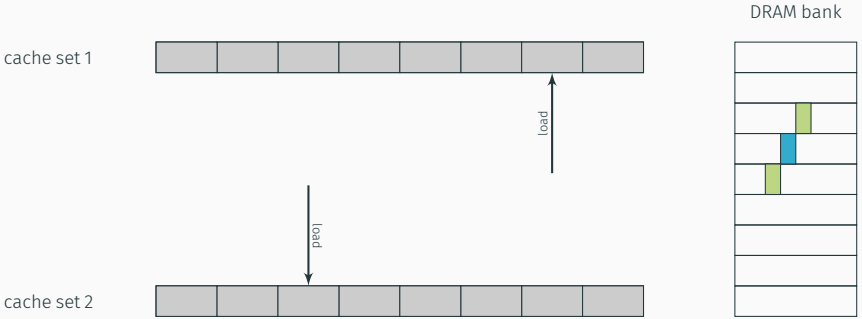

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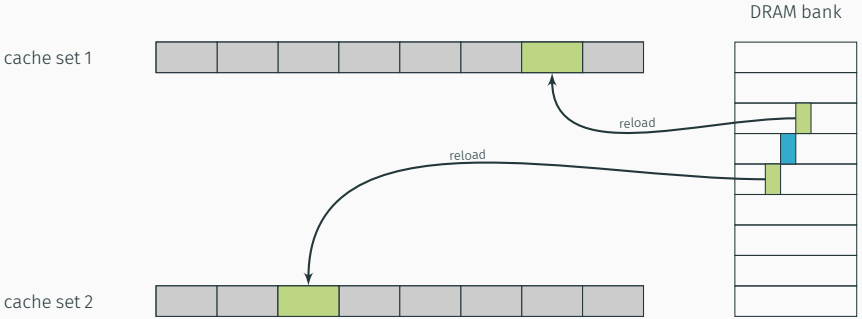

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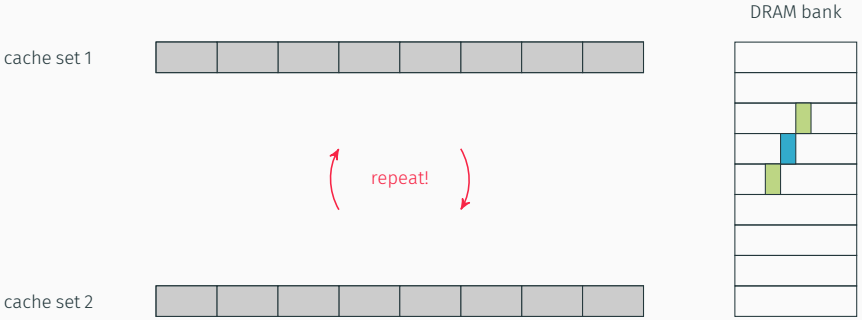

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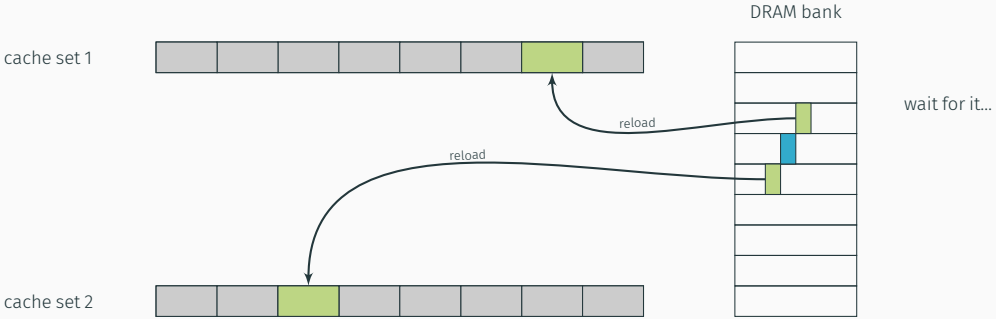

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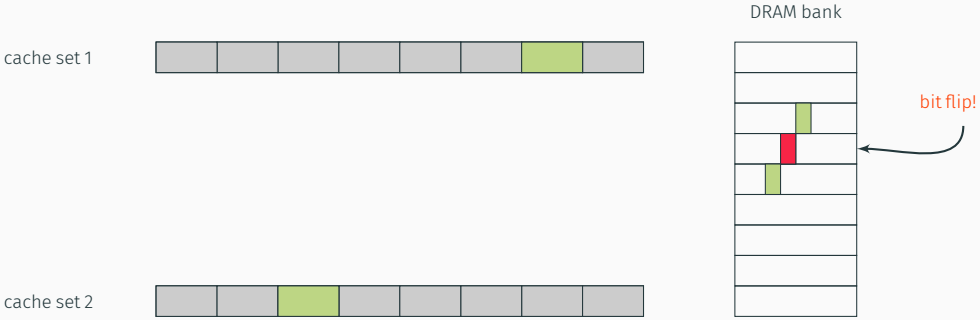
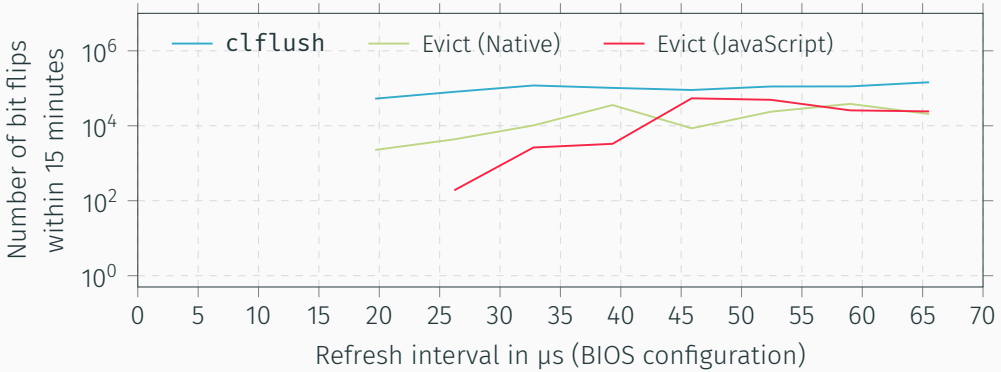


#2 Hammering with cache eviction: Evaluation on Haswell



#3 Hammering with non-temporal accesses

- non-temporal accesses: data accessed just once, not in the future
- NTA instructions $\rightarrow$ bypass cache to minimize cache pollution

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#3 Hammering with non-temporal accesses

```
begin:
  movnti %eax, (X)
  movnti %eax, (Y)

  jmp begin
```

→

```
begin:
  movnti %eax, (X)
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  mov %eax, (X)
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#4 Hammering with uncached memory

Sometimes, everything fails, e.g., on mobile devices

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#4 Hammering with uncached memory

Sometimes, everything fails, e.g., on mobile devices

- ARMv7 flush instruction is privileged
- cache eviction seems to be too slow
- ARMv8 non-temporal stores are still cached in practice

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#4 Hammering with uncached memory

- ION: memory management since Android 4.0
- apps can use `/dev/ion` for uncached, physically contiguous memory
- no privilege and no permission needed

#5 Remote hammering

- previous work: some code execution (even JS)
- how about remote attacks, *i.e.*, triggered by network packets?
  - Tatar et al. use RDMA, fast network communication that does not involve the CPU
  - Lipp et al. use Intel CAT that restricts cache allocation to a subset of cache ways for QoS

Moritz Lipp et al. “Nethammer: Inducing Rowhammer Faults through Network Requests”. In: *arXiv:1805.04956* (2018).

Andrei Tatar et al. “Throwhammer: Rowhammer Attacks over the Network and Defenses”. In: *USENIX ATC 2018*. 2018.

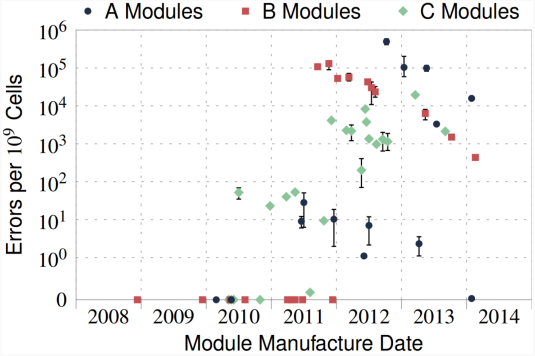
How widespread is the issue?

DDR3:

- Kim et al.: 110/129 modules from 3 vendors, all but 3 since mid-2011
- Seaborn and Dullien: 15/29 laptops

DDR4 believed to be safe:

- still bit flips (Pessl et al.)



Prevalence, by Kim et al.

Peter Pessl et al. "DRAMA: Exploiting DRAM Addressing for Cross-CPU Attacks". In: *USENIX Security Symposium*. 2016.

Yoongu Kim et al. "Flipping bits in memory without accessing them: An experimental study of DRAM disturbance errors". In: *ISCA'14*. 2014.

Issue #2: How do we target accesses?

Physical addresses and DRAM

- fixed map: physical addresses → DRAM cells
- undocumented for Intel

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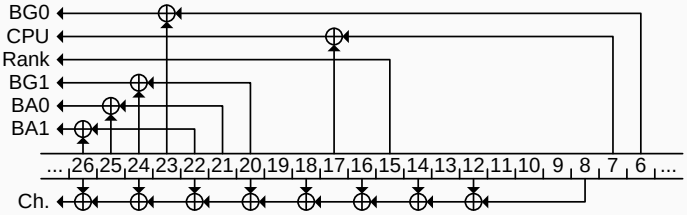

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Memory controller policies

- open-page policy: keep row opened and buffered
  - low latency for subsequent accesses to same row
  - high latency for accesses to any other row

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Memory controller policies

- open-page policy: keep row opened and buffered
  - low latency for subsequent accesses to same row
  - high latency for accesses to any other row

- close-page policy: immediately close row, ready to open a new row
  - medium latency for accesses to any row
  - perform better on multi-core systems

Daniel Gruss et al. "Another Flip in the Wall of Rowhammer Defenses". In: *S&P'18*. 2018.

“Double-sided hammering”

With an open-page policy, you need to alternate accesses to two rows

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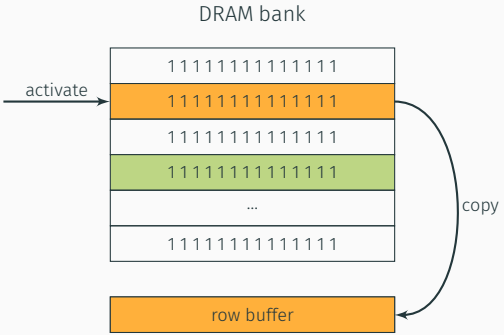

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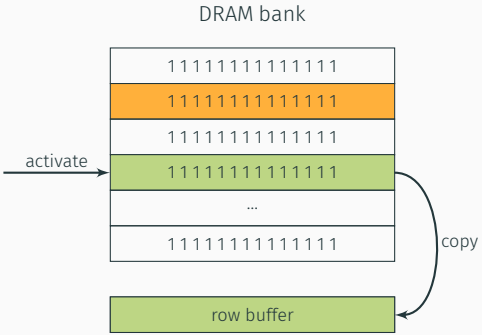

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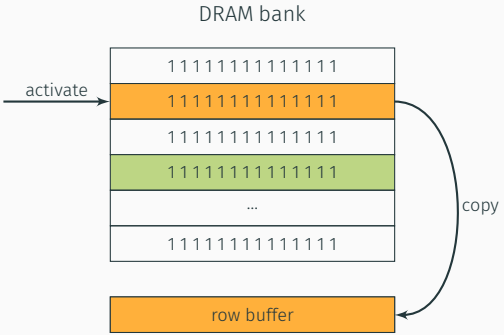

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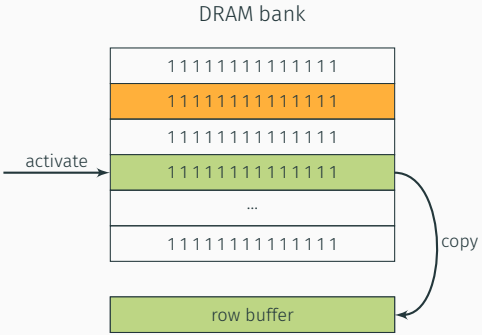

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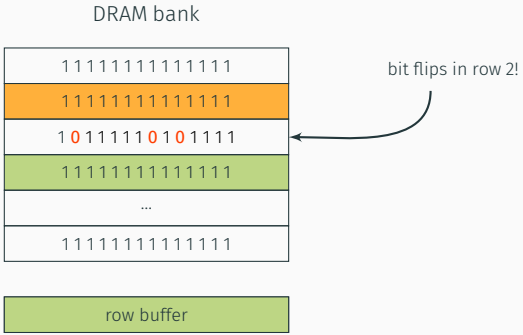

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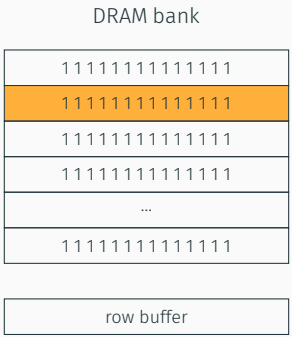
With a close-page policy, you can hammer a single row



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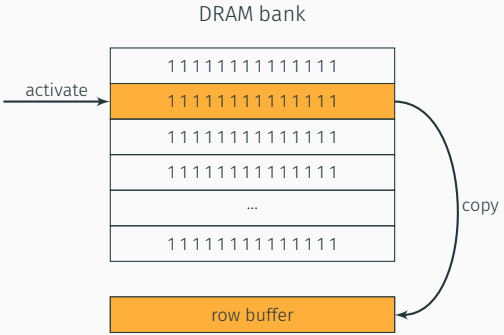

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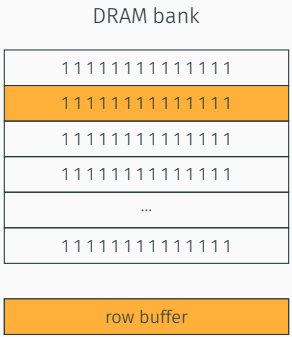

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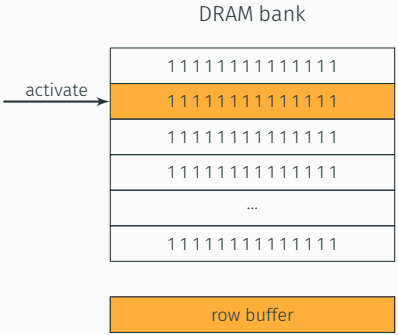

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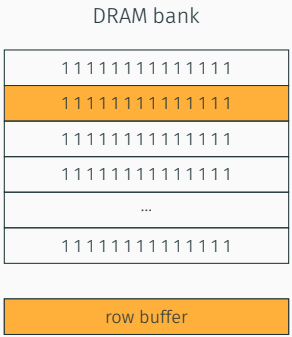

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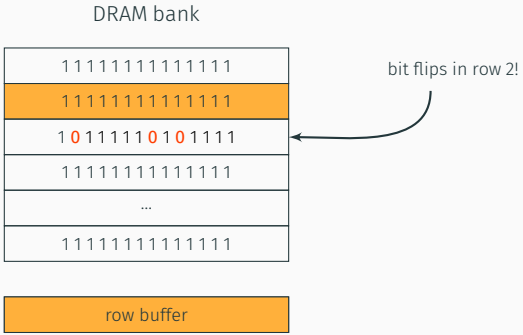

Issue #3: Can we exploit these bit flips?

How to exploit random bit flips?

- Rowhammer was deemed non-exploitable and only a reliability issue

How to exploit random bit flips?

- Rowhammer was deemed non-exploitable and only a reliability issue
- bit flips are not random → highly reproducible flip pattern!
- ideas for exploitation
  1. bit flip in data structure, e.g., page table
  2. bit flip in instruction opcode
  3. bit flip in signature (→ fault-based cryptanalysis)

Bit flips in page tables

General idea

1. allocate a large chunk of memory
2. scan for “good” flips with your own buffer
3. return that particular area of memory to the OS
4. force OS to place data structure there → page tables are good for this
5. trigger bit flip again
6. profit

Mark Seaborn. *Exploiting the DRAM rowhammer bug to gain kernel privileges.* `http://googleprojectzero.blogspot.com/2015/03/exploiting-dram-rowhammer-bug-to-gain.html`. Retrieved on June 26, 2015. 2015.

Bit flips in page tables

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- aim of exploit: get access to a page table
  $\rightarrow$ gives access to all of physical memory
- maximize chances that a bit flip is useful by "spraying" physical memory with page tables

Bit flips in page tables

Page table: 4k page containing array of 512 PTEs (64 bits each)

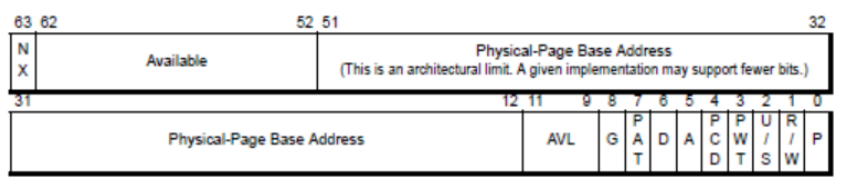

Figure 5-21. 4-Kbyte PTE—Long Mode

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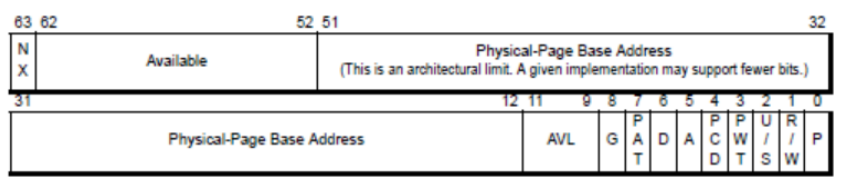

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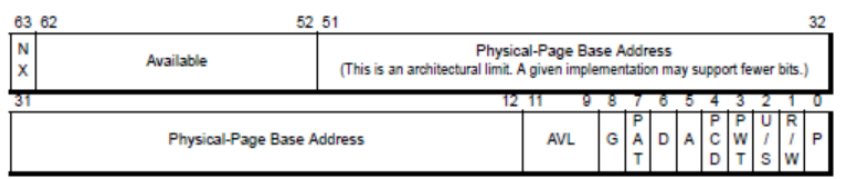
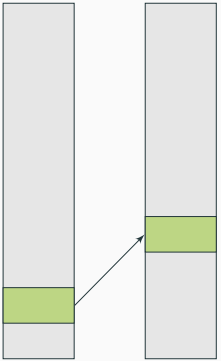


Figure 5-21. 4-Kbyte PTE—Long Mode

Could flip

- "writable" permission bit (RW): 1 bit → 2% chance
- physical page number: 20 bits on 4GB system → 31% chance

Bit flips in page tables

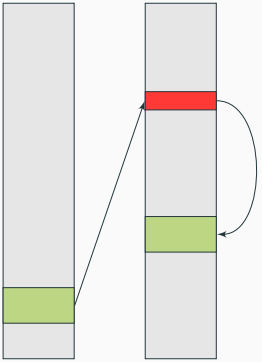


virtual address space

physical memory

- mapping a file with read-write permissions?

Bit flips in page tables



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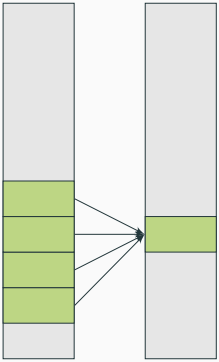

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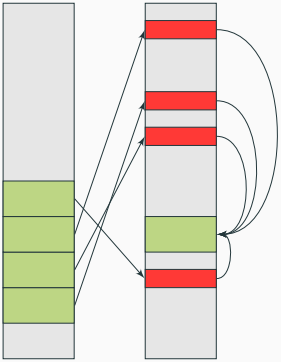
Bit flips in page tables



virtual address space

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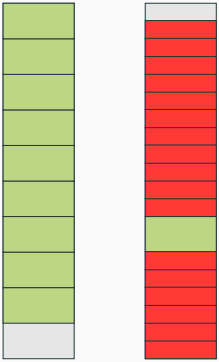
  $\rightarrow$ more PTEs in physical memory!

Bit flips in page tables

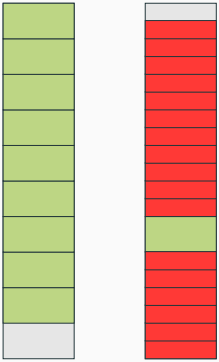


virtual address space

physical memory

- mapping a file with read-write permissions?
  → indirection via page tables
- repeatedly mapping a file with read-write permissions?
  → more PTEs in physical memory!
- we can fill physical memory with PTEs

Bit flips in page tables

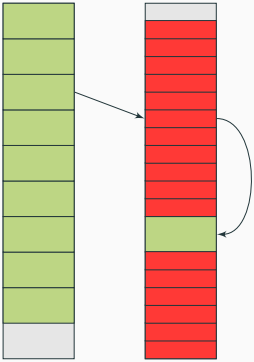


virtual address space

physical memory

- physical memory is filled with PTEs

Bit flips in page tables



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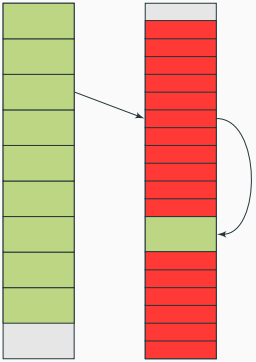

virtual address space

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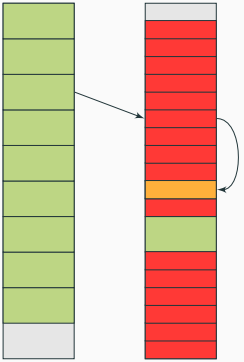
Bit flips in page tables



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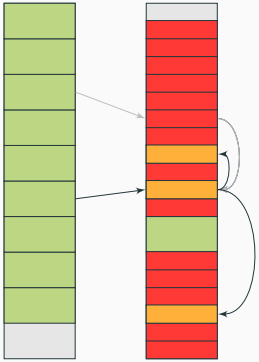

virtual address space

physical memory

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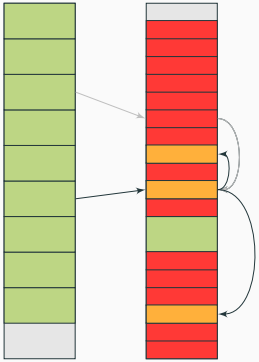
- use that to map any memory read/write

Bit flips in page tables



virtual address space

physical memory

- physical memory is filled with PTEs
- if a bit flips in the right place in the PTE...
- ... the corresponding virtual address now points to a wrong physical page, with RW access, with a great chance the page contains a PT itself
- use that to map any memory read/write
- including kernel memory
  $\rightarrow$ privilege escalation

Bit flips in instruction opcode

- some applications perform actions as root
- can be used by unprivileged users

Daniel Gruss et al. “Another Flip in the Wall of Rowhammer Defenses”. In: *S&P'18*. 2018.

Bit flips in instruction opcode

- some applications perform actions as root
- can be used by unprivileged users
- ping, mount, sudo

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JE

<prefix>

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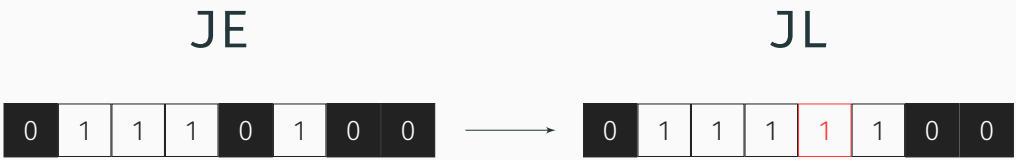

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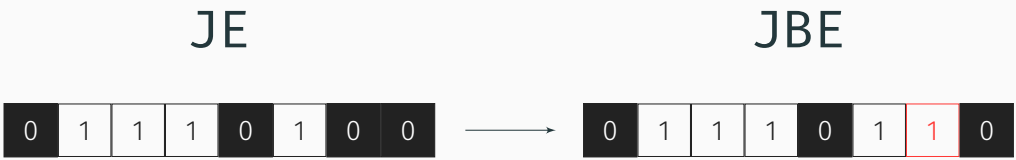

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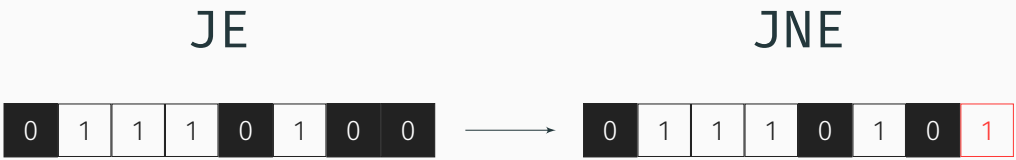

- bit flip in conditional jump → bypass password check

Bit flips in instruction opcode

- not just conditional jump
- other targets include:
  - comparisons
  - addresses of memory loads/stores
- analysis of sudo $\rightarrow$ 29 possible bit flips to bypass password check

Countermeasures

Countermeasures

Different countermeasures have been proposed:

- detection vs prevention
- software vs hardware
- short-term vs long-term

Quick fixes

1. no `clflush` instruction

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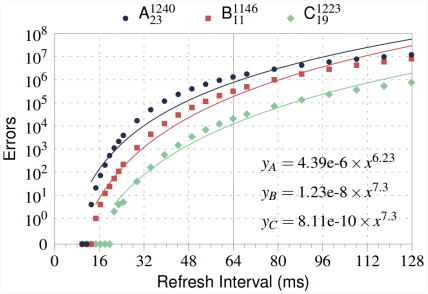
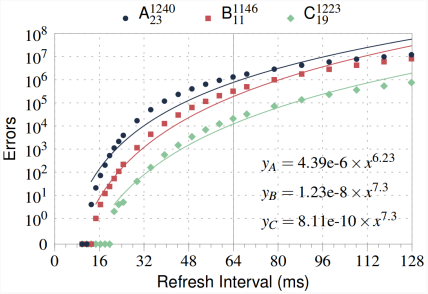


Errors depending on refresh interval ([Kim+14])

Quick fixes

1. no `clflush` instruction → Rowhammer.js
2. increase the refresh rate
   - → would need to be increased by 7× to eliminate all bit flips
   - → implementation: increased by 2× by BIOS vendors



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- ECC protection: server can handle or correct single bit errors

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  - one server did not even halt when bit flips were non-correctable

---

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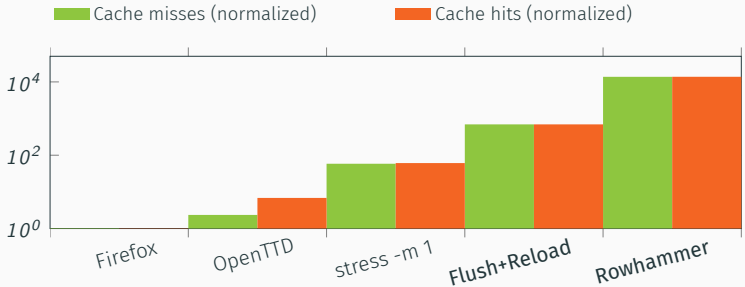
Detecting Rowhammer attacks

- Rowhammer: lots of cache misses that can be monitored with hardware performance counters ([Her+15; Gru+16a; Chi+15; Pay16])



Preventing Rowhammer attacks in hardware (1/3)

Original ideas from [Kim+14]

- making better DRAM chips that are not vulnerable
- using error correcting codes (ECC)
- increasing the refresh rate
- remapping/retiring faulty cells after manufacturing
- identifying hammered rows at runtime and refreshing neighbors

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$\rightarrow$ expensive, performance overhead, or increased power consumption

Preventing Rowhammer attacks in hardware (2/3)

PARA - Probabilistic Adjacent Row Activation ([Kim+14])

- one row closed $\rightarrow$ one adjacent row opened with low probability p

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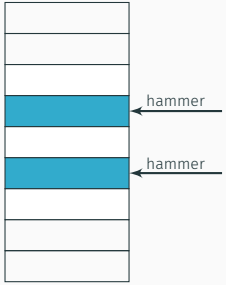
- advantage: stateless $\rightarrow$ not expensive
- for $p = 0.001$ and $N_{th} = 100K$, experiencing one error in one year has a probability 9.4×10^{-14}

Preventing Rowhammer attacks in hardware (3/3)

Target Row Refresh (TRR)

- counter per row
- increment neighbor rows
- refresh when counter reaches a threshold



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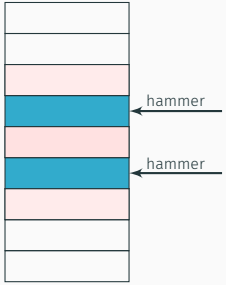

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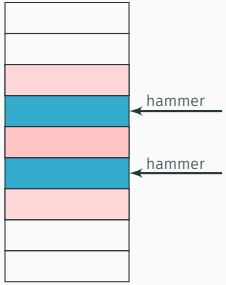

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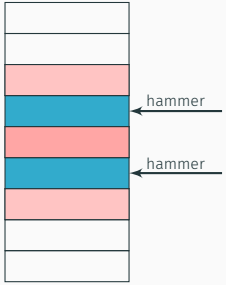

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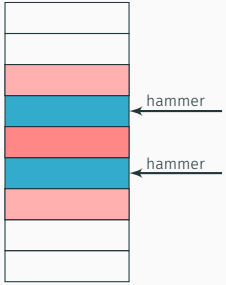

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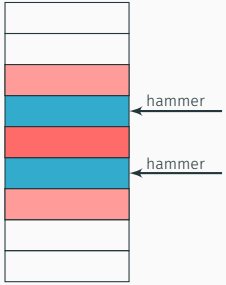

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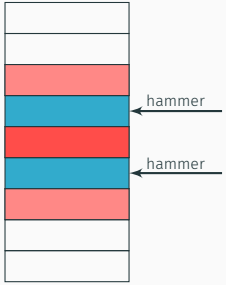

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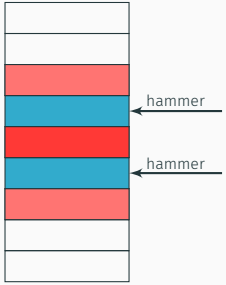

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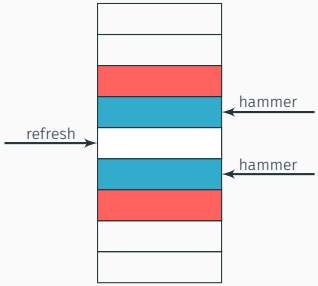

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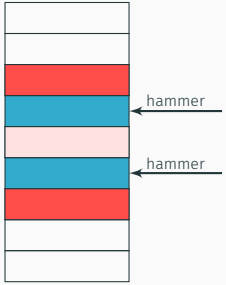

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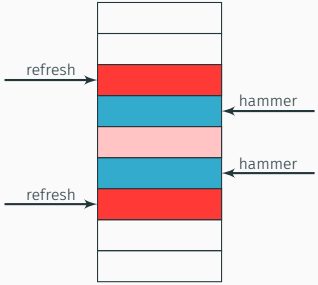

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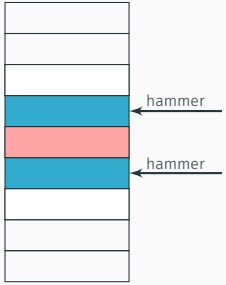

Preventing Rowhammer attacks in software (1/3)

MASCAT: Stopping Microarchitectural Attacks Before Execution (Irazoqui et al.)

- static analysis of the binary
- detect suspicious instruction sequences (`clflush`, `rdtsc`, fences, …)
- open problem: false positives
- since then: remote exploits from network (Lipp et al., Tatar et al.)

Gorka Irazoqui et al. "MASCAT: Stopping Microarchitectural Attacks Before Execution". In: *Cryptology ePrint Archive: Report 2016/1196* (2016).

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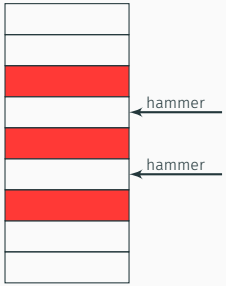

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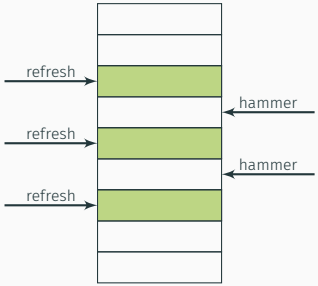

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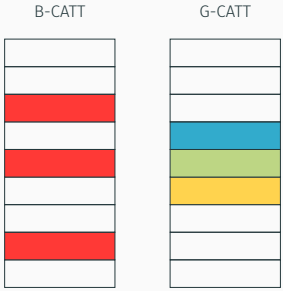
- G-CATT: isolate security domains in physical memory based on potential vulnerability



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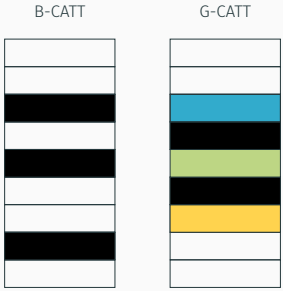

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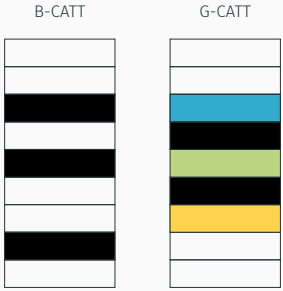

B-CATT: might block 95% of RAM
G-CATT: what about non-kernel or shared pages?
G-CATT: bit flips more than 8 “rows” apart

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Conclusion

- software fault attacks are real, and can be triggered by various techniques in various environments
- no physical access $\rightarrow$ different countermeasures than physical fault attacks
- difficult to replace hardware at a large scale $\rightarrow$ software countermeasures are our best short-term/mid-term hope

Thank you!

Contact

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- @BloodyTangerine

Micro-Architectural Fault Attacks

Clémentine Maurice, CNRS

May 5, 2019—FICHSA, Ben-Gurion University of the Negev, Beer Sheva, Israel

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