Evolution of microarchitectural attacks

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Attacks on micro-architecture

- hardware usually modeled as an abstract layer behaving correctly

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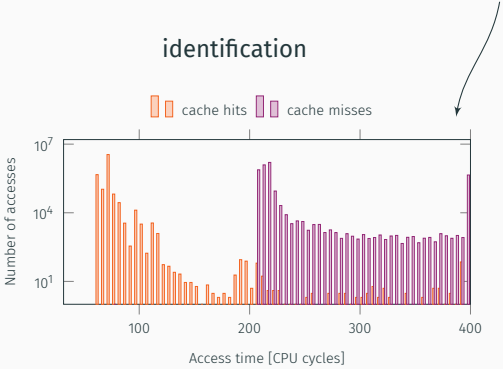

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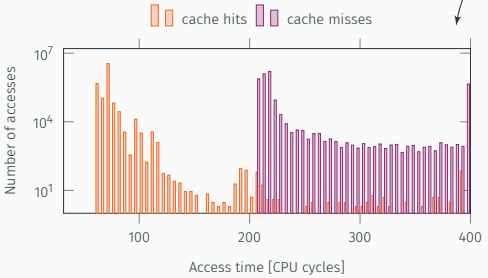
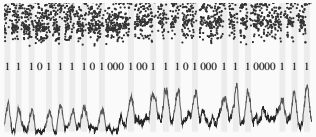
identification

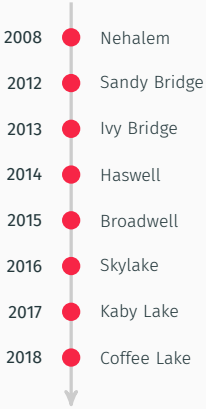


attack



- retrieving secret keys, keystroke timings
- bypassing OS security (ASLR)

From small optimizations...



- new microarchitectures yearly

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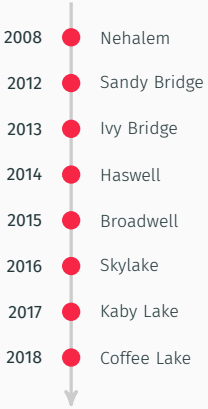

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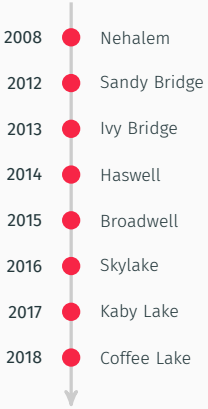

- new microarchitectures yearly
- performance improvement $\approx 5\%$
- very small optimizations: caches, branch prediction...

... To microarchitectural side-channel attacks

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... To microarchitectural side-channel attacks

- microarchitectural side channels come from these optimizations
- several processes are sharing microarchitectural components
- attacker infers information from a victim process via hardware usage
- pure-software attacks by unprivileged processes
- sequences of benign-looking actions $\rightarrow$ hard to detect

Outline

Historical recap of past attacks

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Recent advances

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Historical recap of past attacks

Recent advances

Future and challenges

Historical Recap

From theoretical to practical cache attacks

- first theoretical attack in 1996 by Kocher
- first practical attack on RSA in 2005 by Percival, on AES in 2006 by Osvik et al.
- renewed interest for the field in 2014 after Flush+Reload by Yarom and Falkner

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P. C. Kocher. “Timing Attacks on Implementations of Diffe-Hellman, RSA, DSS, and Other Systems”. In: *Crypto'96*. 1996.

C. Percival. “Cache missing for fun and profit”. In: *Proceedings of BSDCan*. 2005.

D. A. Osvik, A. Shamir, and E. Tromer. “Cache Attacks and Countermeasures: the Case of AES”. In: *CT-RSA 2006*. 2006.

Y. Yarom and K. Falkner. “Flush+Reload: a High Resolution, Low Noise, L3 Cache Side-Channel Attack”. In: *USENIX Security Symposium*. 2014.

Hyper-threading: Same-core attacks

- threads sharing one core share resources: L1, L2 cache, branch predictor

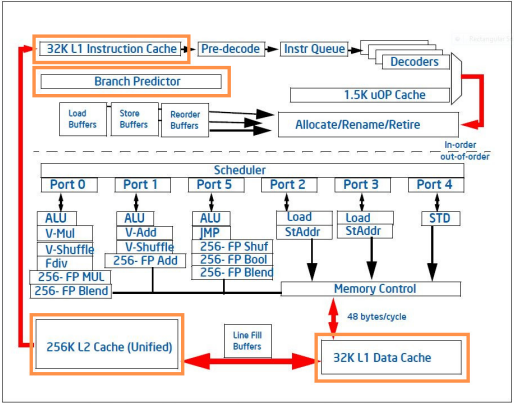

Figure 2-1. Intel microarchitecture code name Sandy Bridge Pipeline Functionality

Easy solution #1

Possible side channels using components shared by a core?

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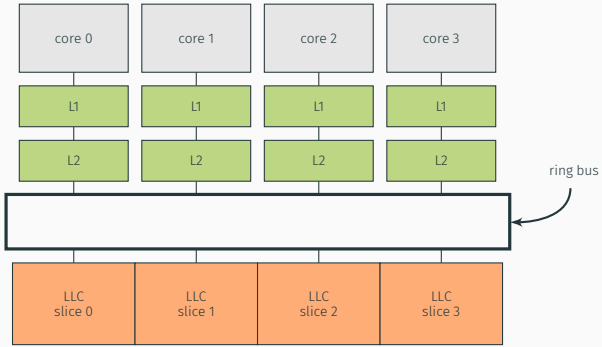
Possible side channels using components shared by a core?

Stop sharing a core!

Caches on Intel CPUs



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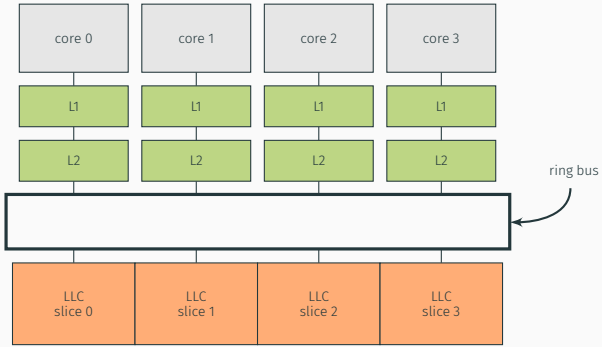

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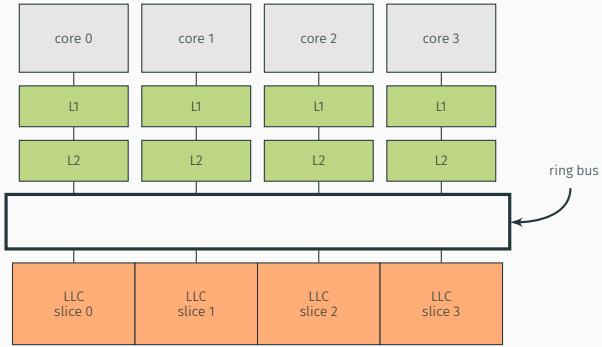

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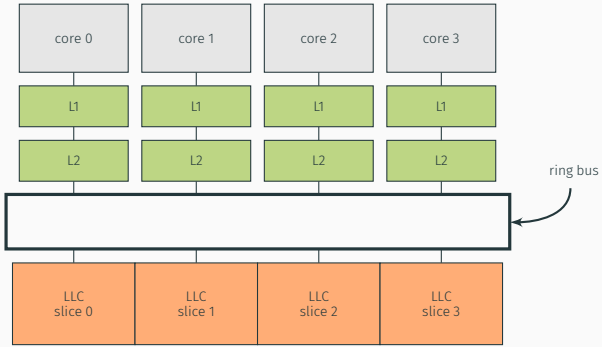

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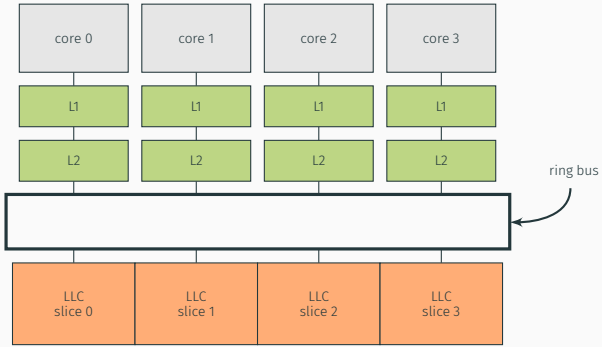

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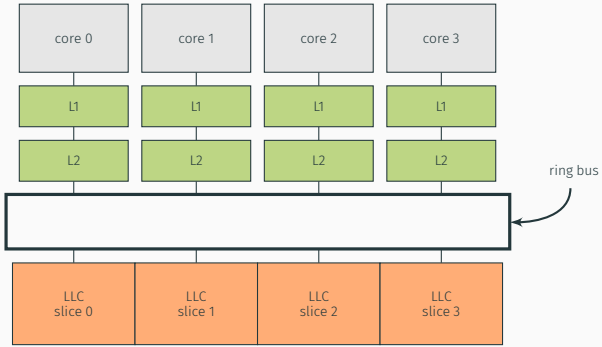

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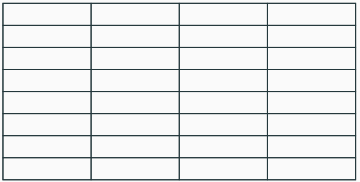
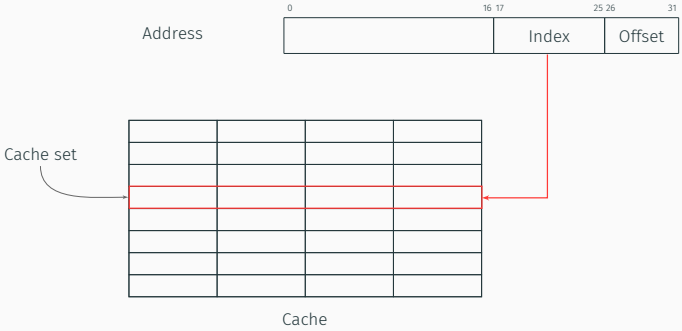
  - shared across cores
  - inclusive

Set-associative caches



Cache

Set-associative caches



Data loaded in a specific set depending on its address

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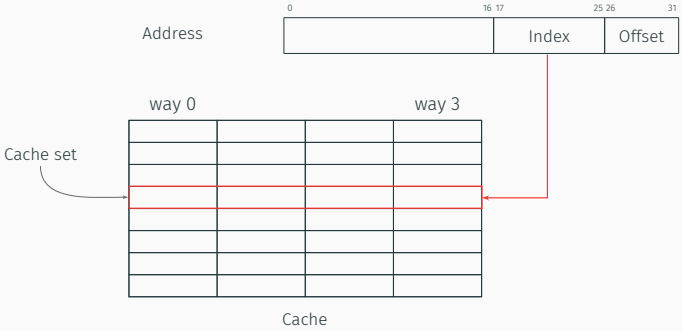

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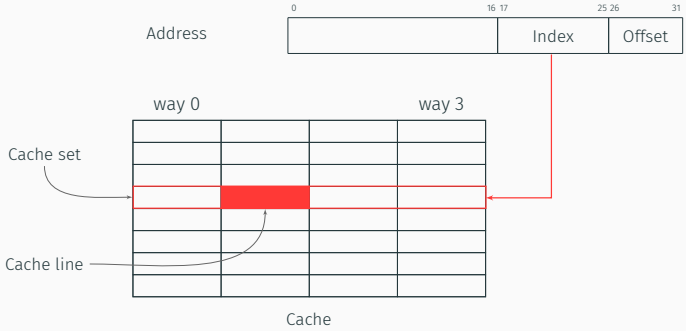

Data loaded in a specific set depending on its address

Several ways per set

Cache line loaded in a specific way depending on the replacement policy

Cache attacks

- caches improve performance

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- SRAM is expensive $\rightarrow$ small caches

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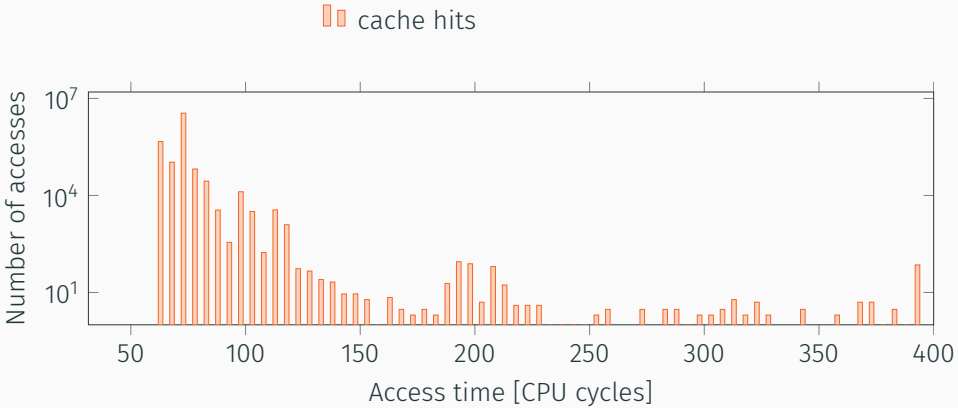
- cache attacks leverage this timing difference

Timing differences



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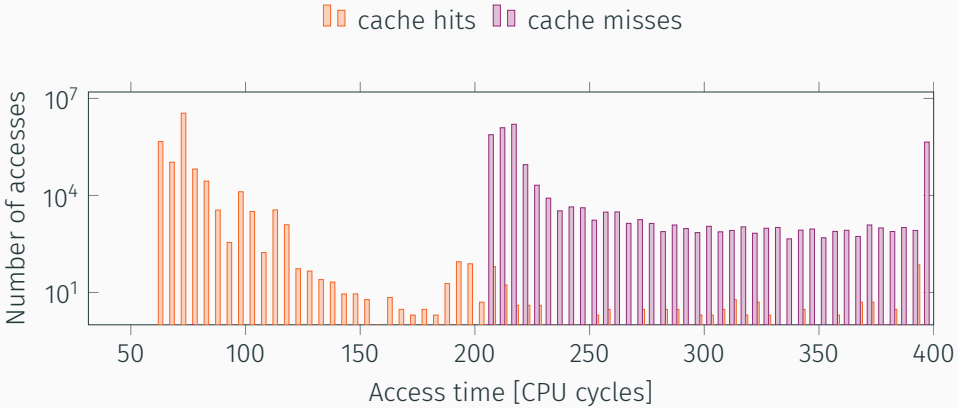
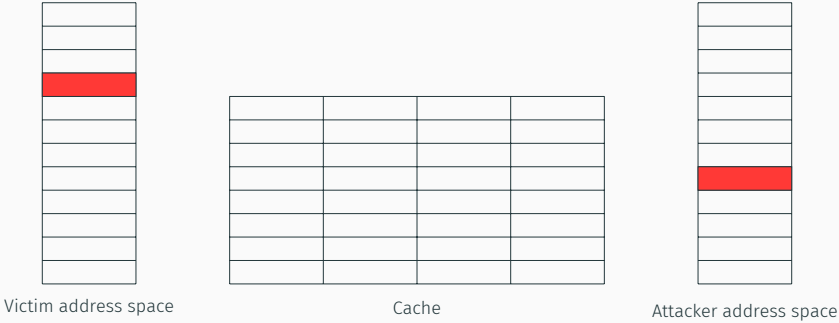


Cache attacks: Flush+Reload



Step 1: Attacker maps shared library (shared memory, in cache)

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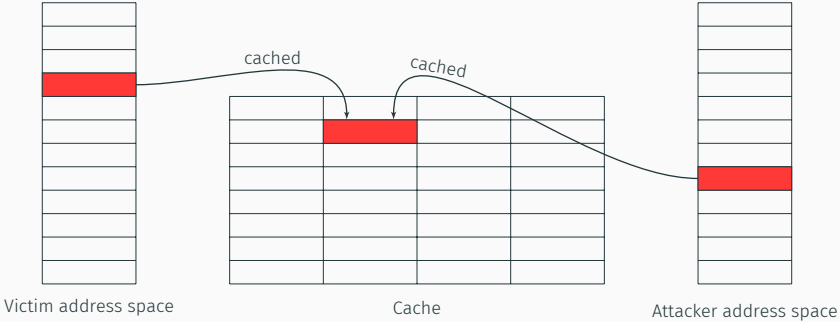

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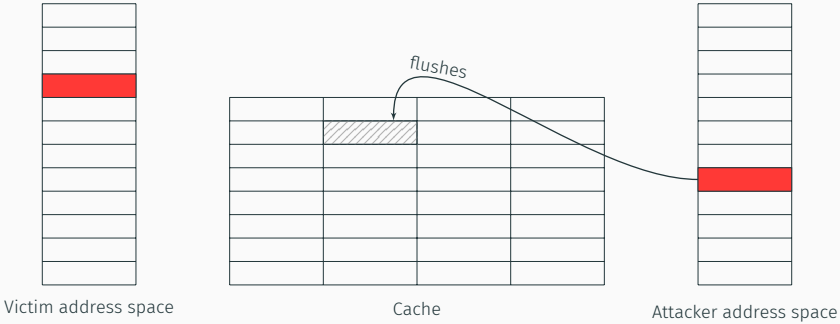

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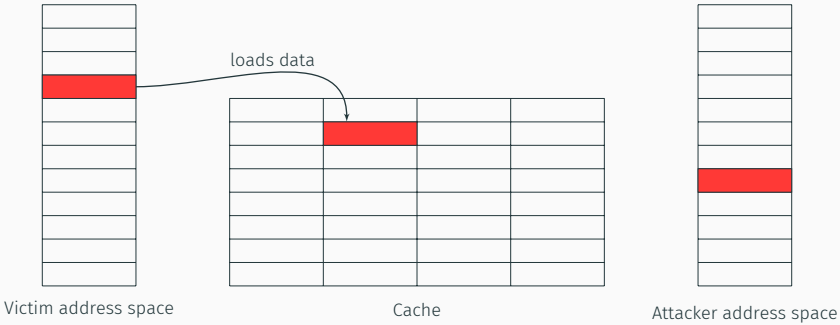

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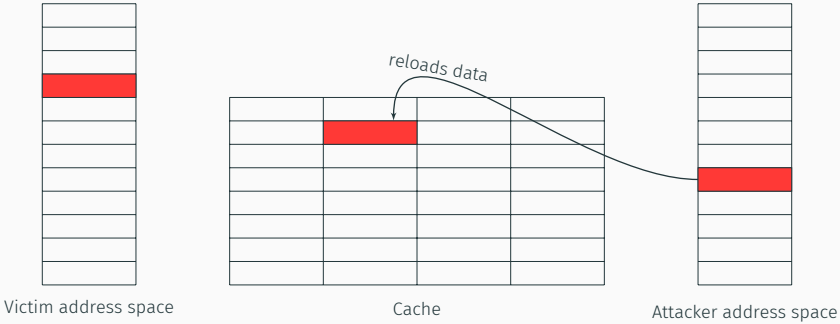

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Step 2: Attacker flushes the shared cache line

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Step 4: Attacker reloads the data

Flush+Reload: Applications

- cross-VM side channel attacks on crypto algorithms
  - RSA: 96.7% of secret key bits in a single signature
  - AES: full key recovery in 30000 dec. (a few seconds)

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`https://github.com/IAIK/cache_template_attacks`

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  - RSA: 96.7% of secret key bits in a single signature
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- Cache Template Attacks: automatically finds information leakage

  → side channel on keystrokes and AES T-tables implementation

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→ memory deduplication between VMs

Easy solution #2

Possible side channels using memory deduplication?

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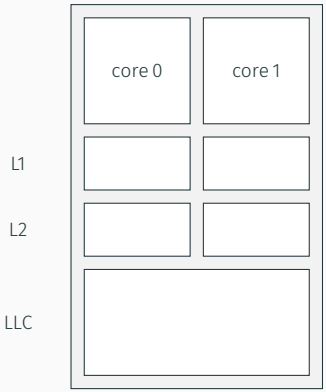
Disable memory deduplication!

Inclusive property



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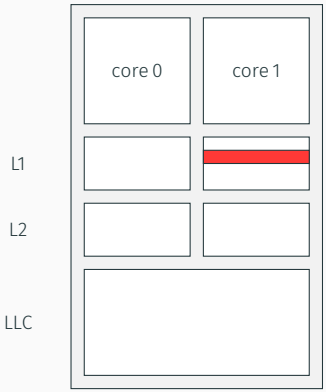

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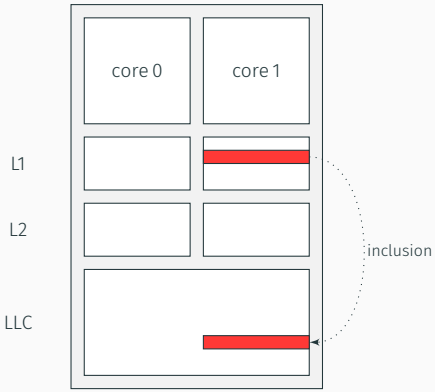

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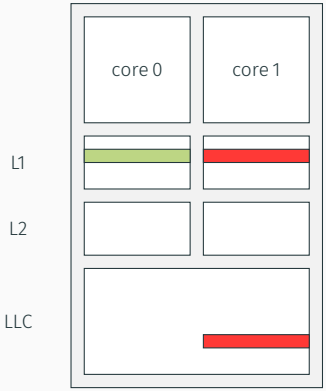

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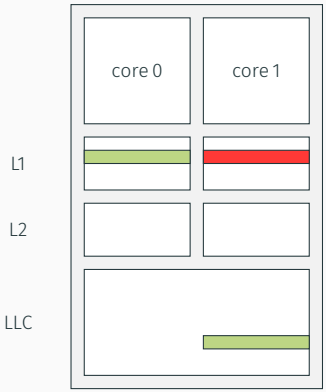

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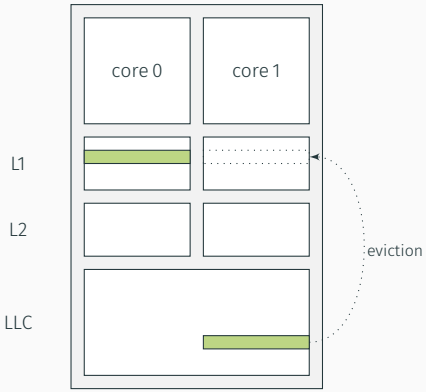

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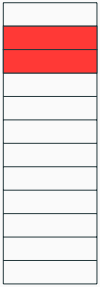
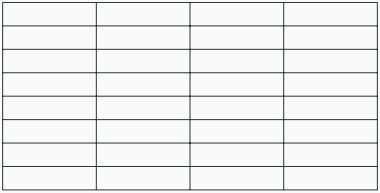
- data evicted from the LLC is also evicted from L1 and L2
- a core can evict lines in the private L1 of another core

Cache attacks: Prime+Probe



Victim address space



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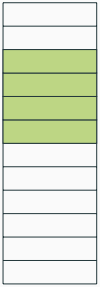

Attacker address space

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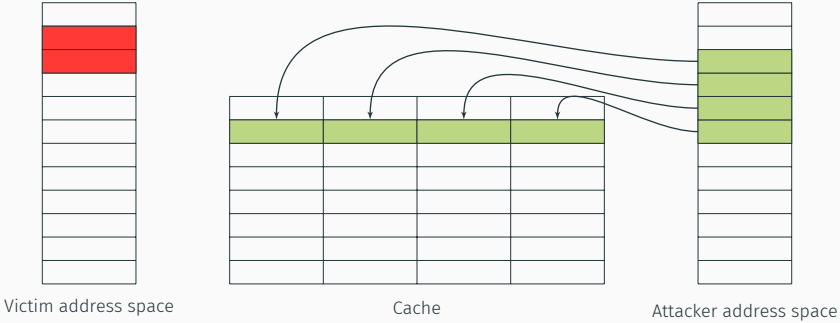

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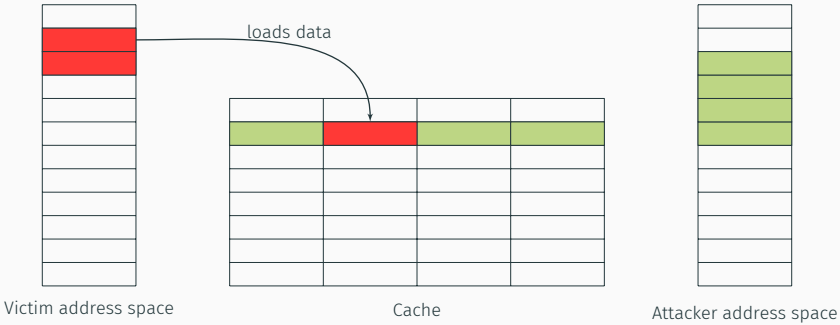

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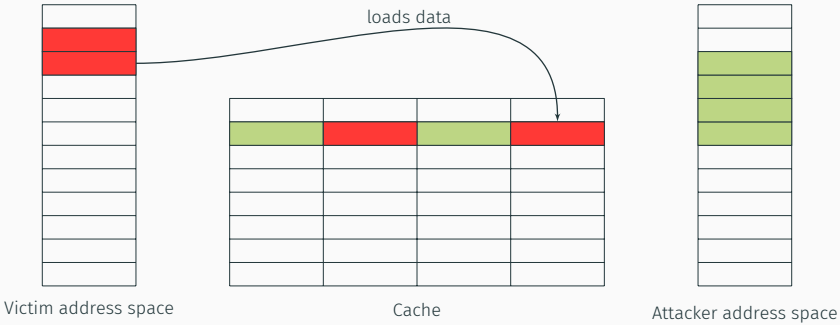

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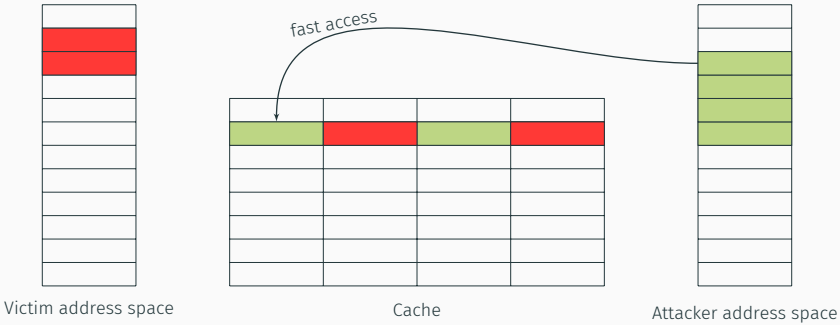

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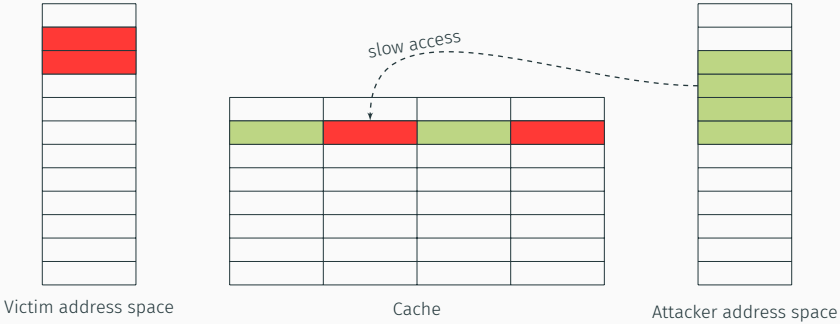

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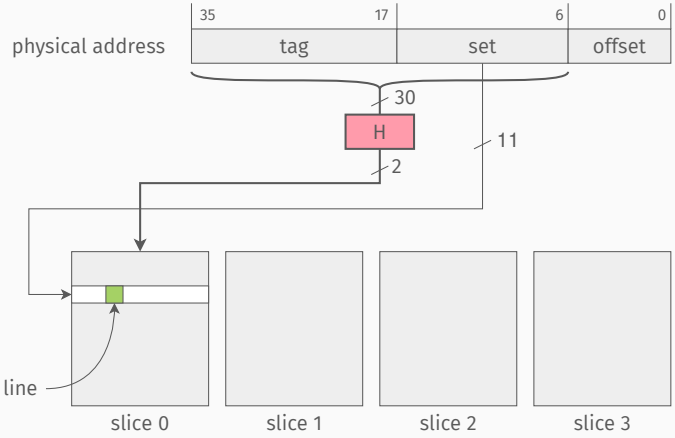
Challenges with Prime+Probe

We need to evict caches lines without `clflush` or shared memory:

1. which addresses do we access to have congruent cache lines?
2. without any privilege?
3. and in which order do we access them?

Last-level cache addressing



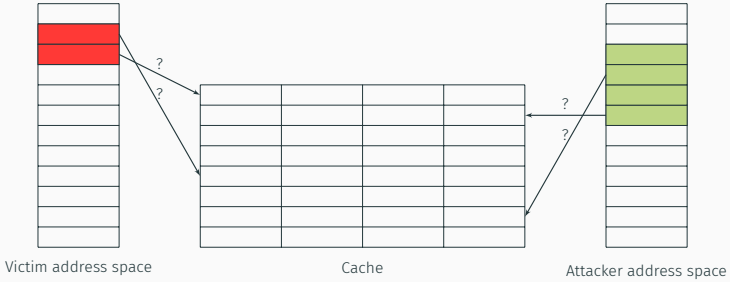
Last-level cache addressing

- last-level cache $\rightarrow$ as many slices as cores
- undocumented hash function that maps a physical address to a slice
- designed for performance

For 2^k slices:

Prime+Probe on recent procesors?

Undocumented function $\rightarrow$ impossible to target a set



C. Maurice, N. Le Scouarnec, C. Neumann, O. Heen, and A. Francillon. “Reverse Engineering Intel Complex Addressing Using Performance Counters”. In: *RAID’15*. 2015

Prime+Probe on recent procesors?

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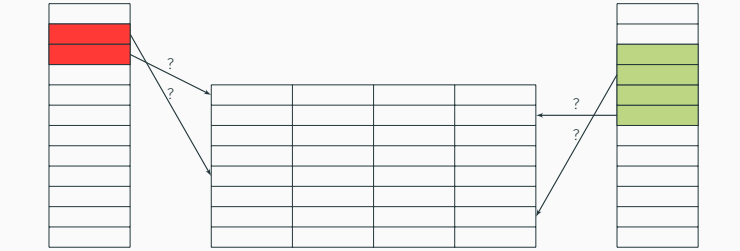

$\rightarrow$ We reverse-engineered the function!

C. Maurice, N. Le Scouarnec, C. Neumann, O. Heen, and A. Francillon. “Reverse Engineering Intel Complex Addressing Using Performance Counters”. In: *RAID'15*. 2015

Prime+Probe: Applications

- cross-VM side channel attacks on crypto algorithms:
  - El Gamal (sliding window): full key recovery in 12 min.
- tracking user behavior in the browser, in JavaScript
- covert channels between virtual machines in the cloud

F. Liu, Y. Yarom, Q. Ge, G. Heiser, and R. B. Lee. “Last-Level Cache Side-Channel Attacks are Practical”. In: *S&P’15*. 2015.

Y. Oren, V. P. Kemerlis, S. Sethumadhavan, and A. D. Keromytis. “The Spy in the Sandbox: Practical Cache Attacks in JavaScript and their Implications”. In: *CCS’15*. 2015.

C. Maurice, M. Weber, M. Schwarz, L. Giner, D. Gruss, C. A. Boano, S. Mangard, and K. Römer. “Hello from the Other Side: SSH over Robust Cache Covert Channels in the Cloud”. In: *NDSS’17*. to appear. 2017.

Easy solution #3

Possible side channels using components shared by a CPU?

Easy solution #3

Possible side channels using components shared by a CPU?

Stop sharing a CPU!?

Recent Advances

Building practical attacks

Covert channels in the cloud

- covert channel: two processes communicating with each other
  - not allowed to do so, e.g., across VMs

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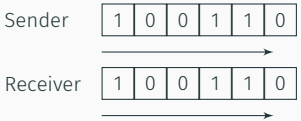
Covert channels in the cloud

- covert channel: two processes communicating with each other
  - not allowed to do so, e.g., across VMs
- literature: stops working with noise on the machine
- solution? “Just use error-correcting codes”

Why can’t we just use error correcting codes?



(a) Transmission without errors

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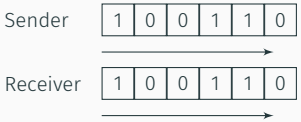

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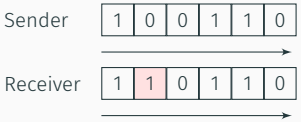

(b) Noise: substitution error

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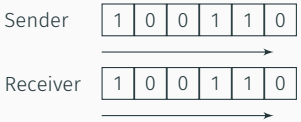

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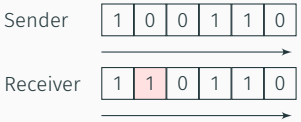

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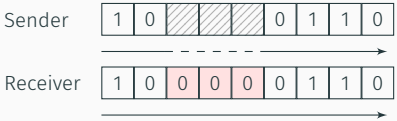

(c) Sender descheduled: insertions

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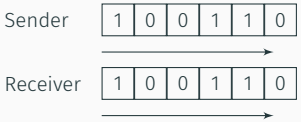

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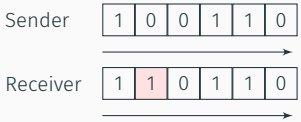

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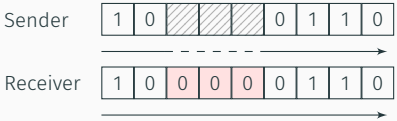

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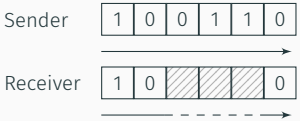

(d) Receiver descheduled: deletions

Our robust covert channel

- physical layer:
  - transmits words as a sequence of ‘0’s and ‘1’s
  - deals with synchronization errors
- data-link layer:
  - divides data to transmit into packets
  - corrects the remaining errors

C. Maurice, M. Weber, M. Schwarz, L. Giner, D. Gruss, C. A. Boano, S. Mangard, and K. Römer. “Hello from the Other Side: SSH over Robust Cache Covert Channels in the Cloud”. In: *NDSS’17*. to appear. 2017

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- sender and receiver agree on one set
- receiver probes the set continuously
- sender transmits ’0’ doing nothing
  → lines of the receiver still in cache → fast access
- sender transmits ’1’ accessing addresses in the set
  → evicts lines of the receiver → slow access

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- need a set of addresses in the same cache set and same slice

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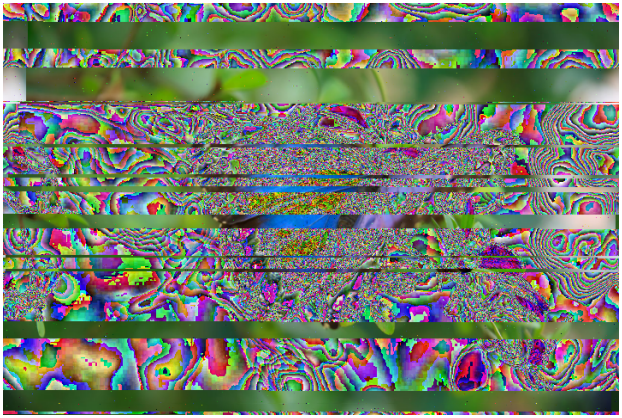
→ we use a jamming agreement

Sending the first image



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- deletion errors: request-to-send scheme that also serves as ack
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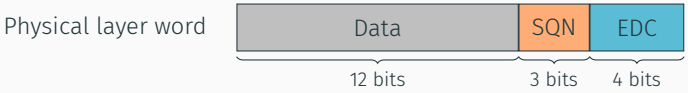
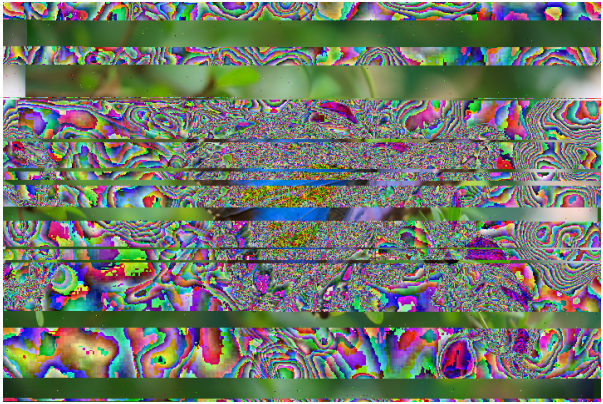
  - 3-bit sequence number
  - request: encoded sequence number (7 bits)
- '0'-insertion errors: error detection code → Berger codes
  - appending the number of '0's in the word to itself

  → property: a word cannot consist solely of '0's



Synchronization (before)



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Data-link layer: Error correction

- Reed-Solomon codes to correct the remaining errors

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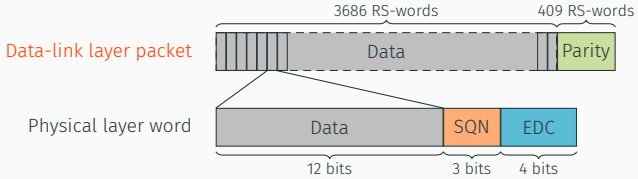
- Reed-Solomon codes to correct the remaining errors
- RS word size = physical layer word size = 12 bits
- packet size = $2^{12} - 1 = 4095$ RS words
- 10% error-correcting code: 409 parity and 3686 data RS words



Error correction (after)

Evaluation

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Native	75.10 KBps	0.00%	–

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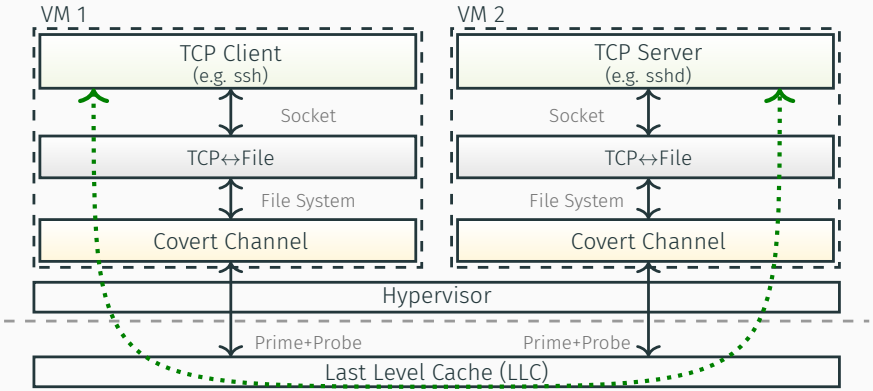
Amazon EC2	45.09 KBps	0.00%	web server serving files on sender VM
Amazon EC2	42.96 KBps	0.00%	`stress -m 2` on sender VM
Amazon EC2	42.26 KBps	0.00%	`stress -m 1` on receiver VM
Amazon EC2	37.42 KBps	0.00%	web server on all 3 VMs, `stress -m 4` on 3rd VM, `stress -m 1` on sender and receiver VMs
Amazon EC2	34.27 KBps	0.00%	`stress -m 8` on third VM

Building an SSH connection



SSH evaluation

Between two instances on Amazon EC2

Noise	Connection
No noise	✓
`stress -m 8` on third VM	✓
Web server on third VM	✓
Web server on SSH server VM	✓
Web server on all VMs	✓
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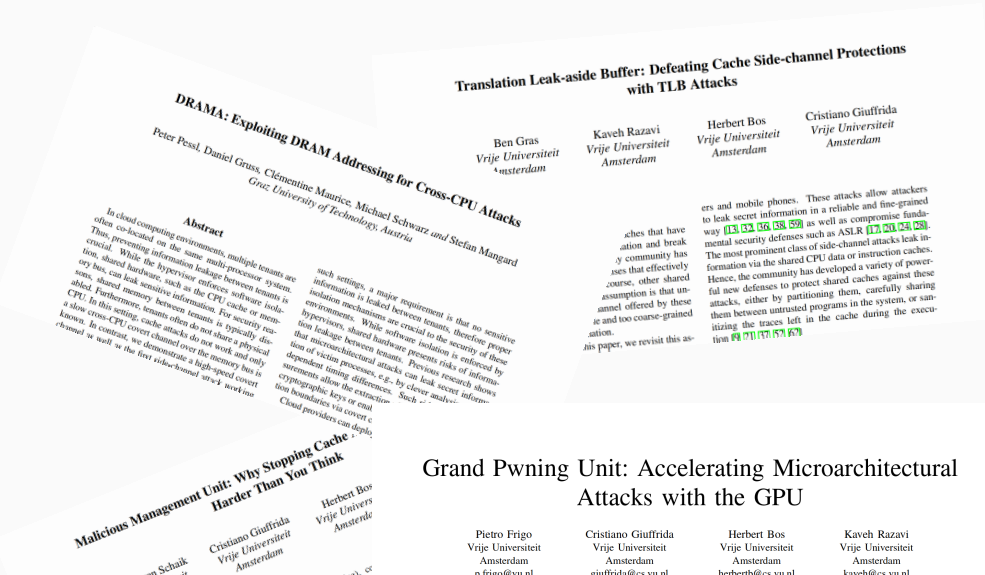
Telnet also works with occasional corrupted bytes with `stress -m 1`

Increasing the attack surface

It's not just caches: Also the DRAM, GPU, MMU, TLB!



Translation Leak-aside Buffer: Defeating Cache Side-channel Protections with TLB Attacks

Ben Gras, Vrije Universiteit Amsterdam
Kaveh Razavi, Vrije Universiteit Amsterdam
Herbert Bos, Vrije Universiteit Amsterdam
Cristiano Giuffrida, Vrije Universiteit Amsterdam

DRAMA: Exploiting DRAM Addressing for Cross-CPU Attacks

Peter Pessl, Daniel Gruss, Clémentine Maurice, Michael Schwarz and Stefan Mangard
Graz University of Technology, Austria

Malicious Management Unit: Why Stopping Cache Attacks in Software is Harder Than You Think

Cristiano Giuffrida, Vrije Universiteit Amsterdam

Grand Pwning Unit: Accelerating Microarchitectural Attacks with the GPU

Pietro Frigo, Vrije Universiteit Amsterdam, p.frigo@vu.nl
Cristiano Giuffrida, Vrije Universiteit Amsterdam, giuffrida@cs.vu.nl
Herbert Bos, Vrije Universiteit Amsterdam, herbertb@cs.vu.nl
Kaveh Razavi, Vrije Universiteit Amsterdam, kaveh@cs.vu.nl

It’s not just native code on x86: Mobile and web too!

ARMageddon: Cache Attacks on Mobile Devices

Moritz Lipp, Daniel Gruss, Raphael Spreitzer, Clémentine Maurice, *and* Stefan Mangard
Graz University of Technology, Austria

Fantastic Timers and Where to Find Them: High-Resolution Microarchitectural Attacks in JavaScript

Michael Schwarz, Clémentine Maurice, Daniel Gruss, and Stefan Mangard
Graz University of Technology, Austria

Practical Keystroke … Sandboxed Jav…

Moritz Lipp, Daniel Gruss, Michael Schwarz, …
Clémentine Maurice, and Stefan Manga…
Graz University of Technology, Austria

The Spy in the Sandbox: Practical Cache Attacks in JavaScript and their Implications

Yossef Oren Vasileios P. Kemerlis Simha Sethumadhavan Angelos D. Keromytis
Columbia University
Department of Computer Science
{yos, vpk, simha, angelosj@cs.columbia.edu

It’s not just side channels: Fault attacks too!

CLKSCREW: Exposing the Perils of Security-Oblivious Energy Management

Adrian Tang, Columbia University
Simha Sethumadhavan, Columbia University
Salvatore Stolfo, Columbia University

Abstract

Rowhammer.js: A Remote Software-Induced Fault Attack in JavaScript

Daniel Gruss, Clémentine Maurice, and Stefan Mangard

Graz University of Technology, Austria

Flipping Bits in Memory Without Accessing Them: An Experimental Study of DRAM Disturbance Errors

Yoongu Kim Ross Daly* Jeremie Kim Chris Fallin* Ji Hye Lee
Donghyuk Lee Chris Wilkerson Konrad Lai Onur Mutlu

Carnegie Mellon University Intel Labs

Abstract. Memory isolation is a key property of a reliable and secure computing system — an access to one memory address should not have unintended side effects on data stored in other addresses. However, as DRAM process technology scales down to smaller dimensions, it becomes more difficult to prevent DRAM cells from electrically interacting with each other. In this paper, we expose the vulnerability of commodity

disturbance errors, DRAM manufacturers have been employing a two-pronged approach: (i) improving inter-cell isolation through circuit-level techniques [22, 32, 49, 61, 73] and (ii) screening for disturbance errors during post-production testing [3, 4, 64]. We demonstrate that their efforts to contain disturbance errors have not always been successful, and that erroneous DRAM chips have been slipping into the field.[1]

Future and Challenges

Challenges and questions

- lack of documentation on microarchitectural components
- which components are vulnerable to these attacks?
- which software is vulnerable to these attacks?
- how to prevent attacks based on performance optimizations without removing performance?

Future: More transient execution attacks?

It's not just code that is executed!

- Meltdown breaks isolation between applications and kernel by exploiting Out-of-Order execution
- Spectre mistrains branch prediction to speculatively execute code that should not be executed
- 3 initial variants in January, as of today 21 variants

C. Canella, J. Van Bulck, M. Schwarz, M. Lipp, B. von Berg, P. Ortner, F. Piessens, D. Evtyushkin, and D. Gruss. "A Systematic Evaluation of Transient Execution Attacks and Defenses". In: *arXiv preprint arXiv:1811.05441* (2018)

Conclusion

- first paper by Kocher in 1996: 22 years of research in this area
- domain still in expansion: increasing number of papers published since 2015
- adopted countermeasures mainly target cryptographic implementations
- still a lot more to discover on this iceberg :)
- quick fixes don't work
- still a lot more work needed to find satisfying countermeasures

Thank you!

Contact

- clementine.maurice@irisa.fr
- @BloodyTangerine

Evolution of microarchitectural attacks

Clémentine Maurice, CNRS, IRISA

December 11, 2018–WOS 8