Introduction to cache side-channel attacks

Clémentine Maurice, CNRS, IRISA

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Who am I

- **Clémentine Maurice**
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- IRISA lab, EMSEC group
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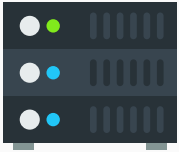
- @BloodyTangerine

Scope

Everyday hardware: servers, workstations, laptops, smartphones...



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→ crypto and sensitive info., e.g., keystrokes and mouse movements

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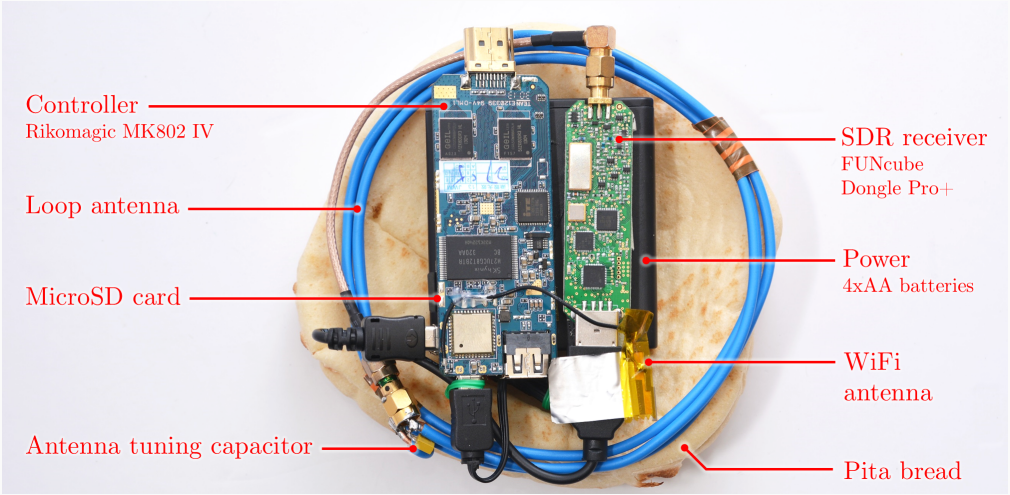

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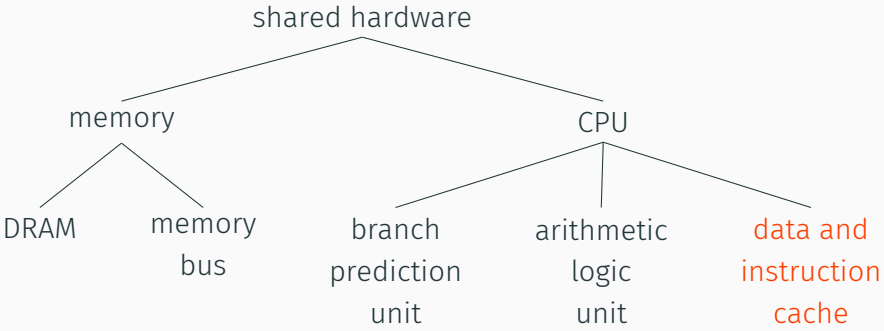
  → targeted attacks, physical access
- via shared hardware and microarchitecture
  → “remote” attacks, no physical access to the device

Shared hardware



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- no documentation on this intellectual property

Today's CPU complexity

- "Intel x86 documentation has more pages than the 6502 has transistors"

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Outline

- Background on cache attacks
- Reverse-engineering
- Practical attacks
- Countermeasures and open challenges
- Conclusion

Background on cache attacks

MOV—Move

Opcode	Instruction	Op/ En	64-Bit Mode	Compat/ Leg Mode	Description
88 /r	MOV *r/m8,r8*	MR	Valid	Valid	Move *r8* to *r/m8*.
REX + 88 /r	MOV *r/m8****,*r8****	MR	Valid	N.E.	Move *r8* to *r/m8*.
89 /r	MOV *r/m16,r16*	MR	Valid	Valid	Move *r16* to *r/m16*.
89 /r	MOV *r/m32,r32*	MR	Valid	Valid	Move *r32* to *r/m32*.
REX.W + 89 /r	MOV *r/m64,r64*	MR	Valid	N.E.	Move *r64* to *r/m64*.
8A /r	MOV *r8,r/m8*	RM	Valid	Valid	Move *r/m8* to *r8*.
REX + 8A /r	MOV *r8****,*r/m8****	RM	Valid	N.E.	Move *r/m8* to *r8*.
8B /r	MOV *r16,r/m16*	RM	Valid	Valid	Move *r/m16* to *r16*.
8B /r	MOV *r32,r/m32*	RM	Valid	Valid	Move *r/m32* to *r32*.
REX.W + 8B /r	MOV *r64,r/m64*	RM	Valid	N.E.	Move *r/m64* to *r64*.
8C /r	MOV *r/m16,Sreg***	MR	Valid	Valid	Move segment register to *r/m16*.
REX.W + 8C /r	MOV *r/m64,Sreg***	MR	Valid	Valid	Move zero extended 16-bit segment register to *r/m64*.
8E /r	MOV *Sreg,r/m16***	RM	Valid	Valid	Move *r/m16* to segment register.
REX.W + 8E /r	MOV *Sreg,r/m64***	RM	Valid	Valid	Move *lower 16 bits of r/m64* to segment register.
A0	MOV AL,*moffs8**	FD	Valid	Valid	Move byte at (*seg:offset*) to AL.
REX.W + A0	MOV AL,*moffs8**	FD	Valid	N.E.	Move byte at (*offset*) to AL.
A1	MOV AX,*moffs16**	FD	Valid	Valid	Move word at (*seg:offset*) to AX.
A1	MOV EAX,*moffs32**	FD	Valid	Valid	Move doubleword at (*seg:offset*) to EAX.
REX.W + A1	MOV RAX,*moffs64**	FD	Valid	N.E.	Move quadword at (*offset*) to RAX.

mov

64-Bit Mode Exceptions

#GP(0)	If the memory address is in a non-canonical form.
	If an attempt is made to load SS register with NULL segment selector when CPL = 3.
	If an attempt is made to load SS register with NULL segment selector when CPL < 3 and CPL ≠ RPL.
#GP(selector)	If segment selector index is outside descriptor table limits.
	If the memory access to the descriptor table is non-canonical.
	If the SS register is being loaded and the segment selector's RPL and the segment descriptor's DPL are not equal to the CPL.
	If the SS register is being loaded and the segment pointed to is a nonwritable data segment.
	If the DS, ES, FS, or GS register is being loaded and the segment pointed to is not a data or readable code segment.
	If the DS, ES, FS, or GS register is being loaded and the segment pointed to is a data or nonconforming code segment, but both the RPL and the CPL are greater than the DPL.
#SS(0)	If the stack address is in a non-canonical form.
#SS(selector)	If the SS register is being loaded and the segment pointed to is marked not present.
#PF(fault-code)	If a page fault occurs.
#AC(0)	If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD	If attempt is made to load the CS register.
	If the LOCK prefix is used.

`mov`—What could go wrong?

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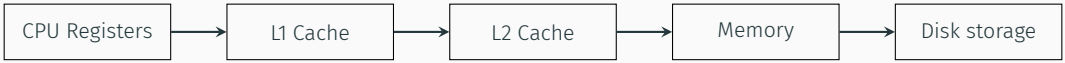
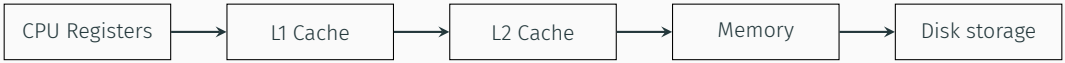
→ side effects on computations!

Memory hierarchy



- data can reside in

Memory hierarchy



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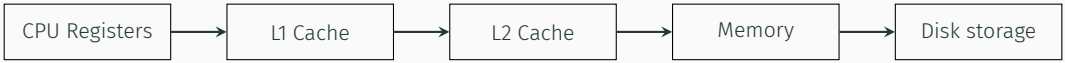

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  - different levels of the CPU cache

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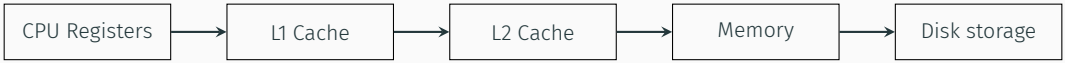

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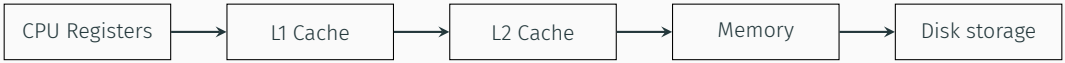
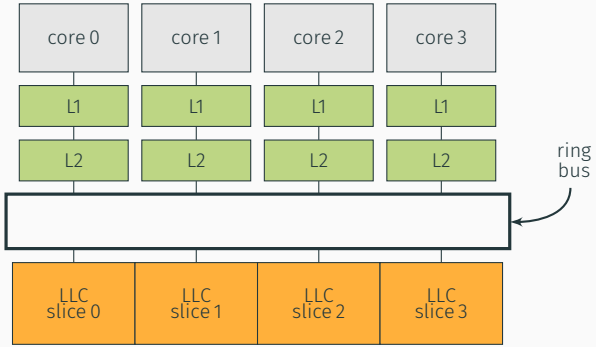


- data can reside in
  - CPU registers
  - different levels of the CPU cache
  - main memory
  - disk storage

Caches on Intel CPUs



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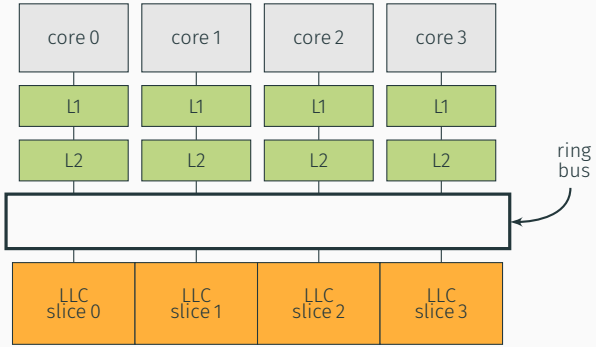

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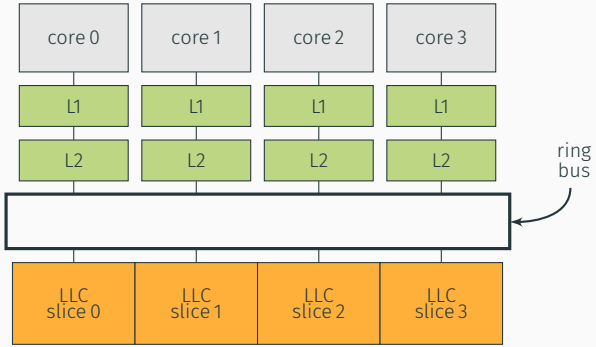

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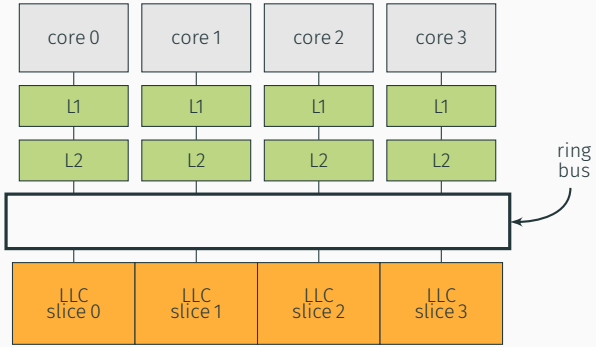

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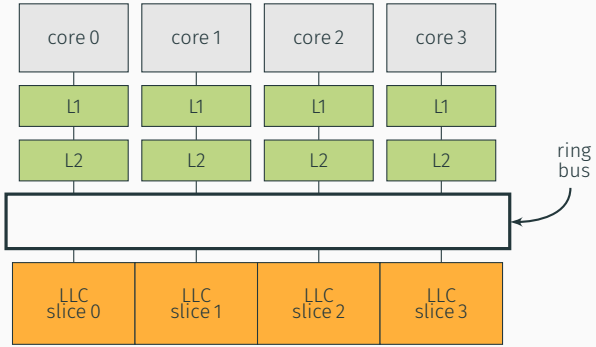
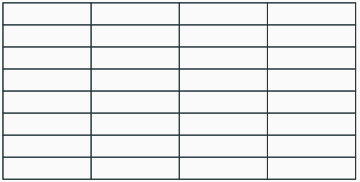


- L1 and L2 are private
- last-level cache
  - divided in slices
  - shared across cores
  - inclusive

Set-associative caches



Cache

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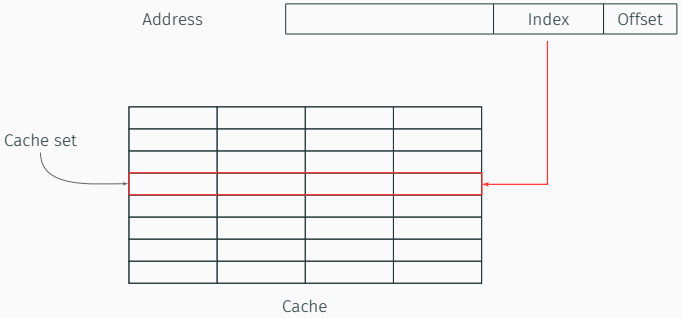

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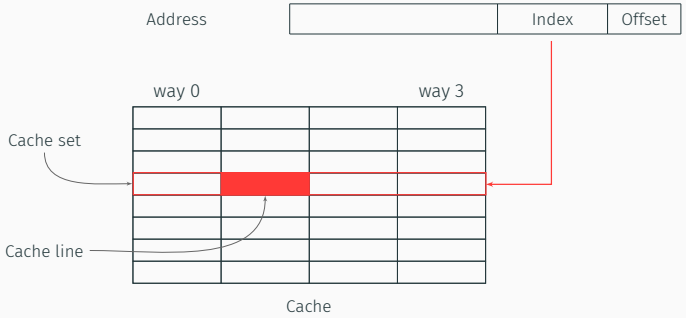
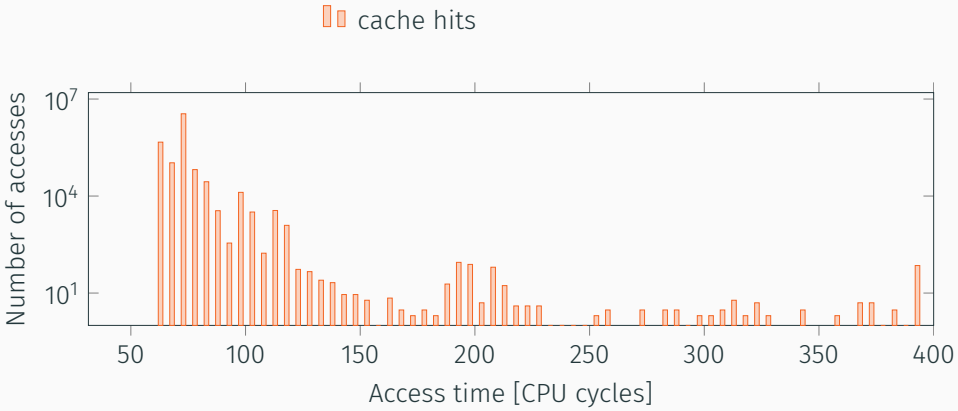


Data loaded in a specific set depending on its address

Several ways per set

Cache line loaded in a specific way depending on the replacement policy

Timing differences



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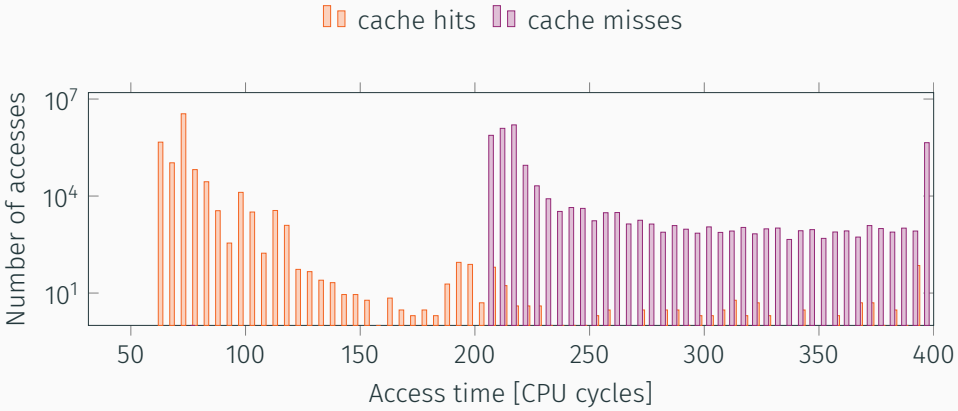

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- attacker monitors which lines are accessed, not the content
- covert channel: two processes communicating with each other
  - not allowed to do so, e.g., across VMs
- side-channel attack: one malicious process spies on benign processes
  - e.g., steals crypto keys, spies on keystrokes

Cache attacks techniques

- two (main) techniques
  1. Flush+Reload (Gullasch et al., Osvik et al., Yarom et al.)
  2. Prime+Probe (Percival, Osvik et al., Liu et al.)
- exploitable on x86 and ARM

D. Gullasch et al. “Cache Games – Bringing Access-Based Cache Attacks on AES to Practice”. In: *S&P’11*. 2011.

Y. Yarom et al. “Flush+Reload: a High Resolution, Low Noise, L3 Cache Side-Channel Attack”. In: *USENIX Security Symposium*. 2014.

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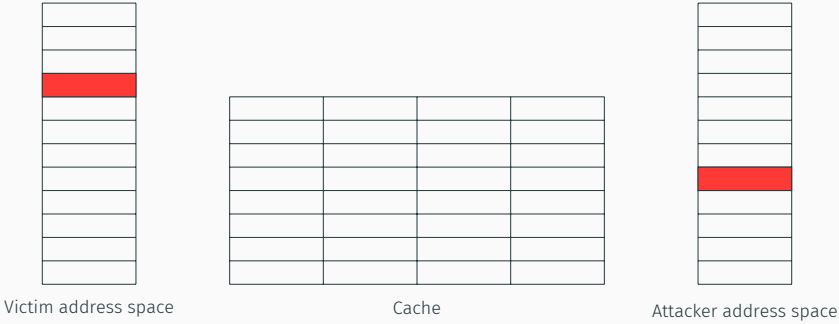
Cache attacks: Flush+Reload



Step 1: Attacker maps shared library (shared memory, in cache)

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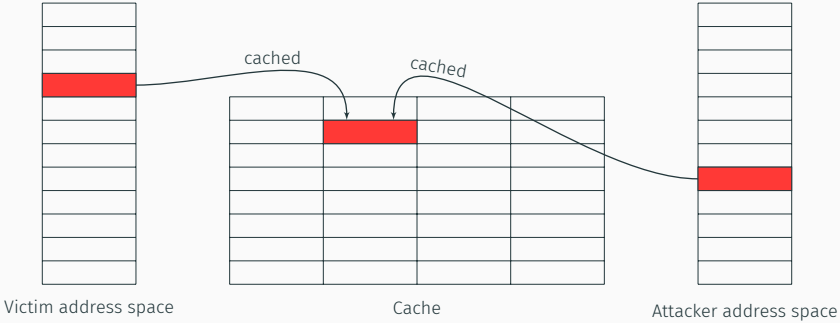

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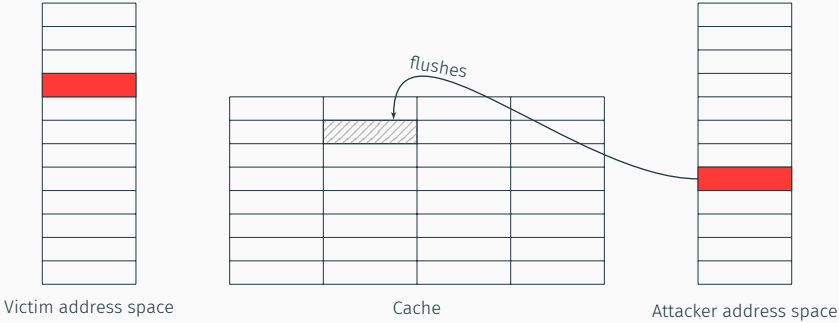

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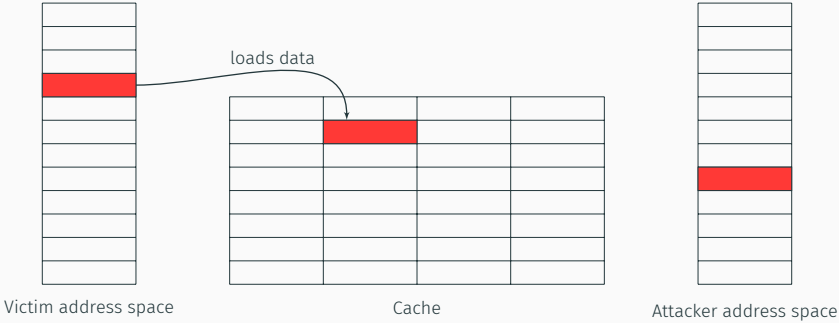

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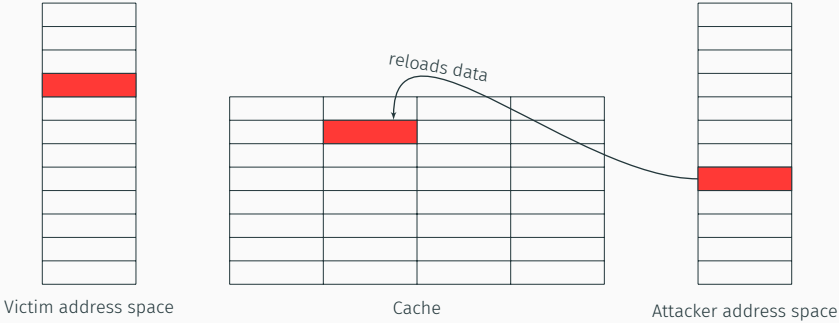

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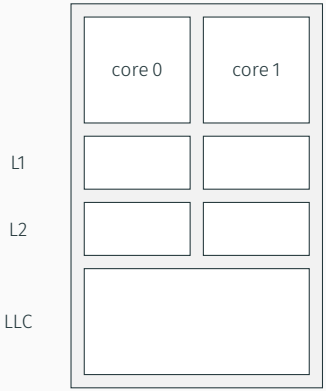
Step 4: Attacker reloads the data

What if there is no shared memory?

Inclusive property



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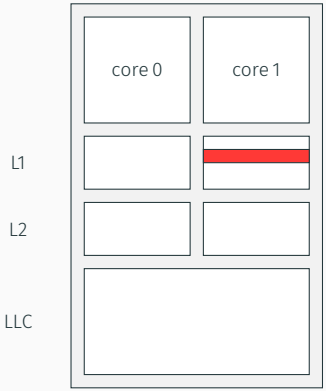

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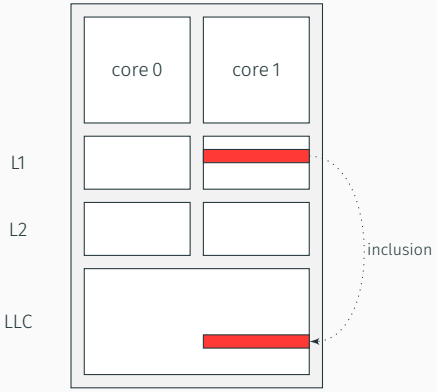

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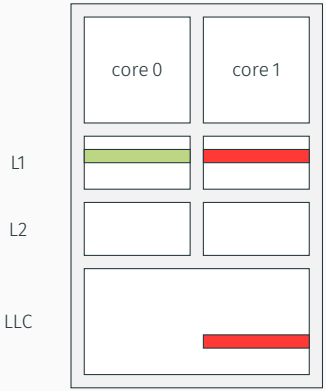

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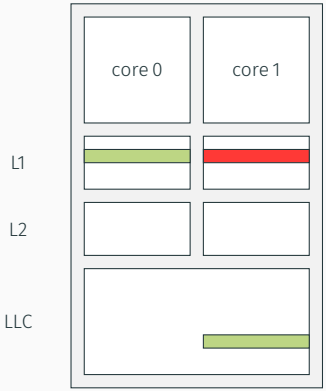

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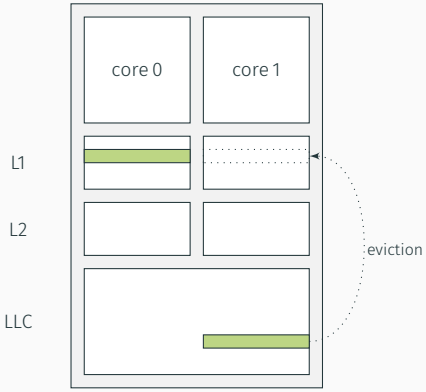

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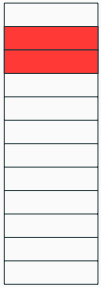
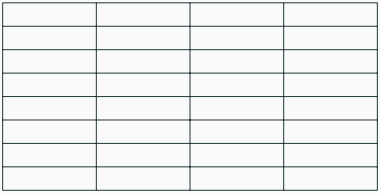
- a core can evict lines in the private L1 of another core

Cache attacks: Prime+Probe



Victim address space



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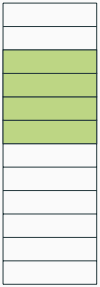
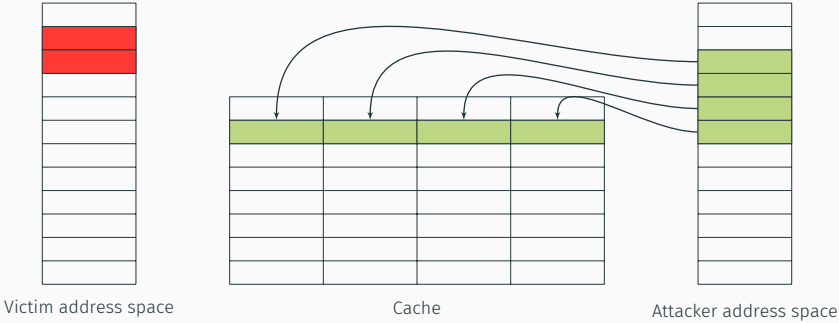


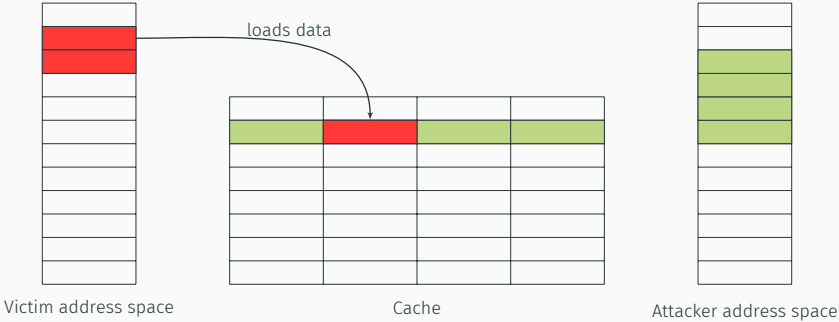
Attacker address space

Cache attacks: Prime+Probe



Step 1: Attacker primes, *i.e.*, fills, the cache (no shared memory)

Cache attacks: Prime+Probe



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Step 2: Victim evicts cache lines while running

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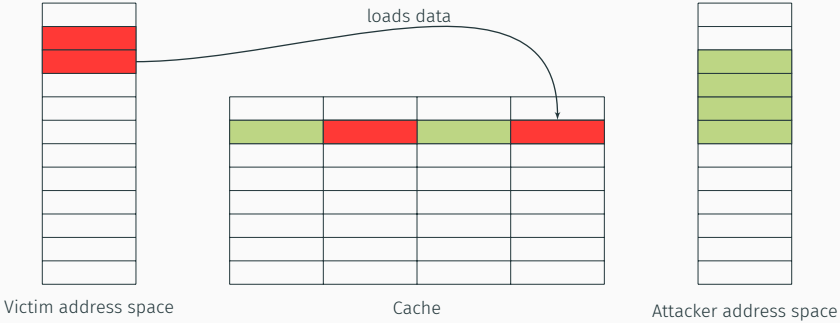

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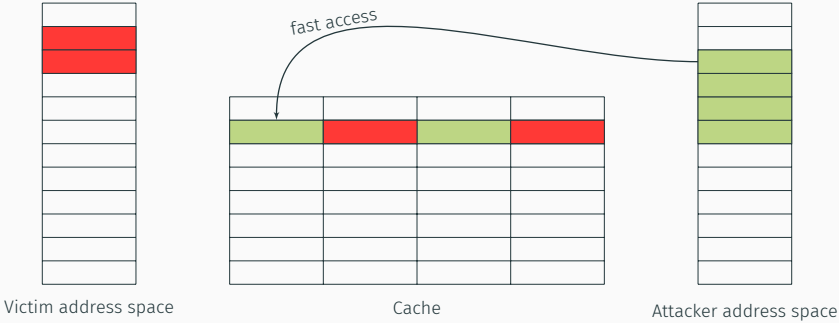

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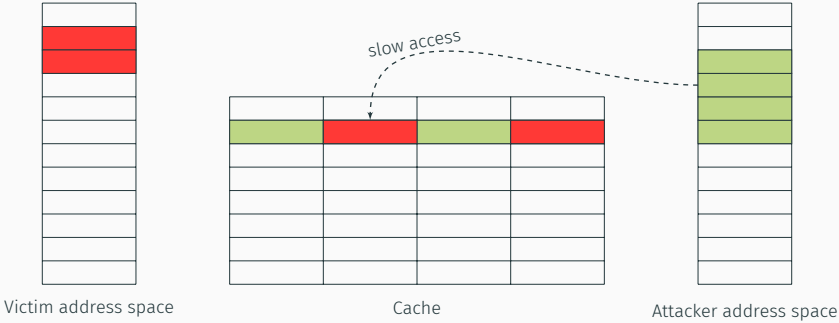
Step 3: Attacker probes data to determine if set has been accessed

Cache attacks: Prime+Probe



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Challenges with Prime+Probe

We need to evict caches lines without `clflush` or shared memory:

1. which addresses do we access to have congruent cache lines?
2. without any privilege?
3. and in which order do we access them?

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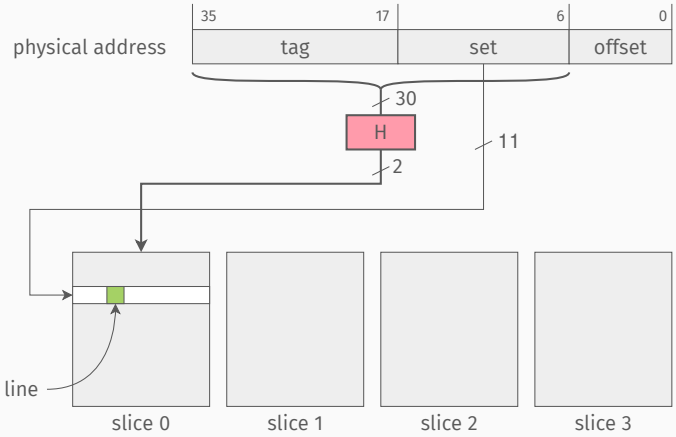
Last-level cache addressing



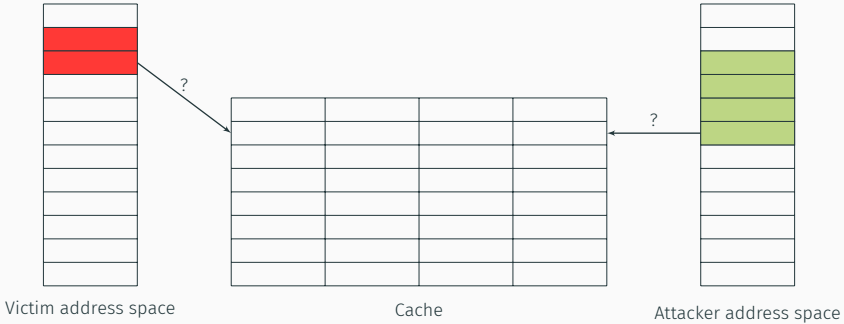
Last-level cache addressing

- last-level cache $\rightarrow$ as many slices as cores
- undocumented hash function that maps a physical address to a slice
- designed for performance

For 2^k slices:

Prime+Probe on recent processors?

Undocumented function $\rightarrow$ impossible to target the same set in the same slice



Reverse-engineering last-level cache

Reverse engineering method

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Reverse engineering method

1. find some way to map one address to one slice
2. repeat for every address with a 64B stride
3. infer a function out of it

How to map addresses to slices?

- with performance counters (Maurice et al., 2015)
- with a timing attack
  - using `clflush` (using Gruss et al., 2016)
  - using memory accesses (Yarom et al., 2015)

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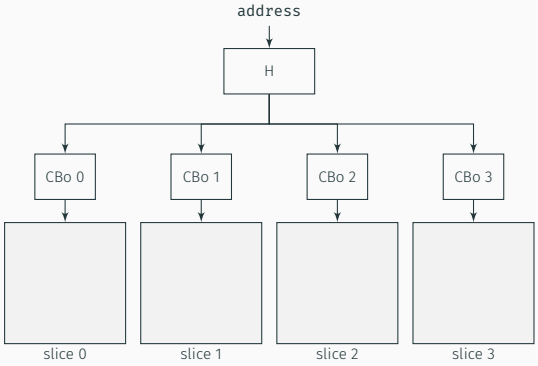
C. Maurice et al. “Reverse Engineering Intel Complex Addressing Using Performance Counters”. In: *RAID’15*. 2015

Mapping with performance counters

- event UNC_CBO_CACHE_LOOKUP counts accesses to a slice



UNC_CBO_CACHE_LOOKUP	0	0	0	0

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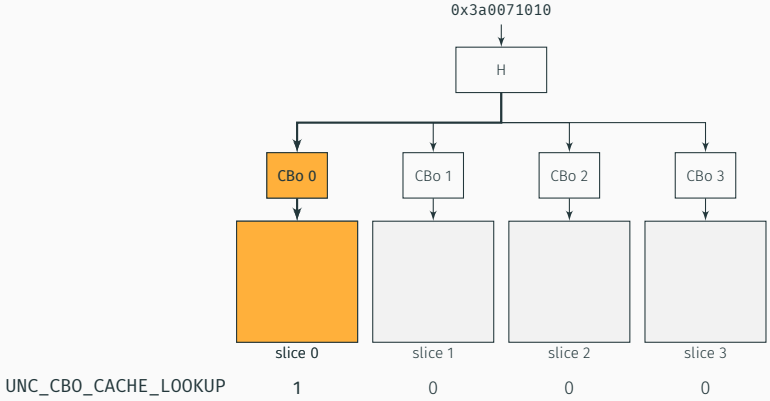

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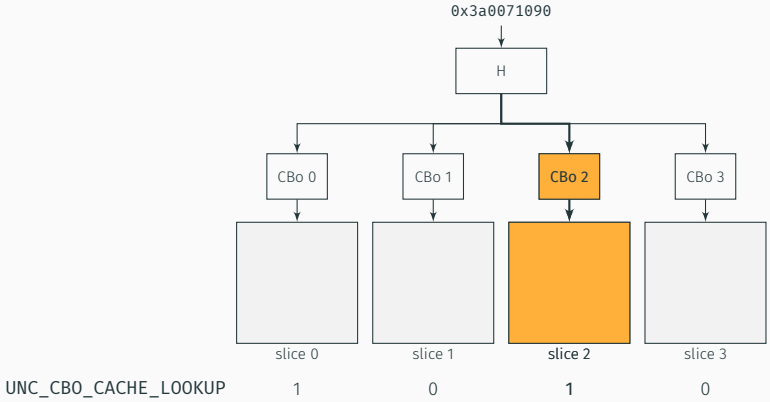

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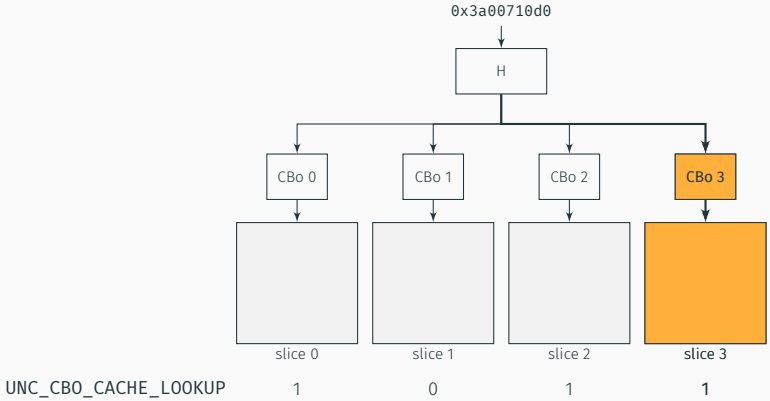

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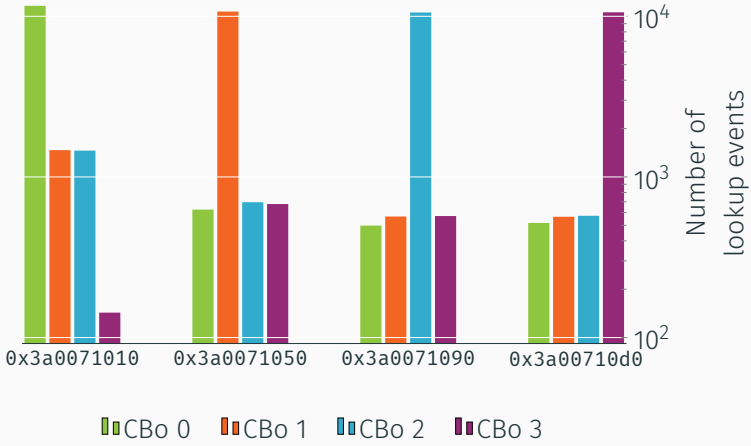
5. slice is the one that has the maximum lookup events

Mapping physical addresses to slices



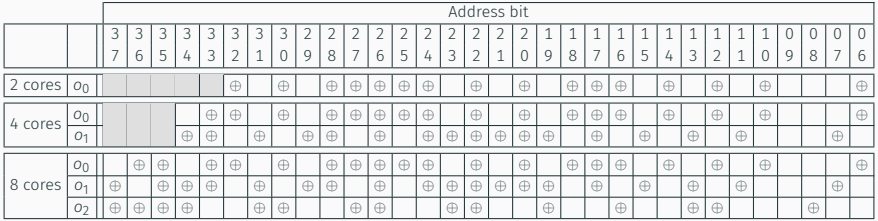
Inferring the function

Two cases:

1. 2^n number of cores: linear function $\rightarrow$ XORs of address bits
   - solve the linear equation
   - or brute force (not that long)
2. the remainder: non-linear function

Last-level cache linear functions

3 functions, depending on the number of cores



Function valid for Sandy Bridge, Ivy Bridge, Haswell, Broadwell

Practical applications

Covert channels in the cloud

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  - not allowed to do so, e.g., across VMs

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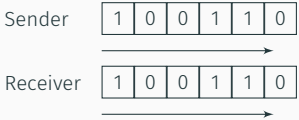
Covert channels in the cloud

- covert channel: two processes communicating with each other
  - not allowed to do so, e.g., across VMs
- literature: stops working with noise on the machine
- solution? “Just use error-correcting codes”

Why can’t we just use error correcting codes?



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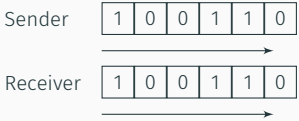

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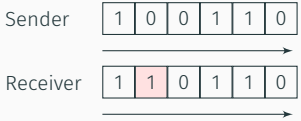

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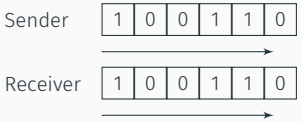

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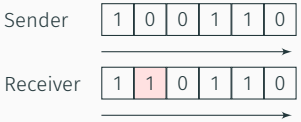

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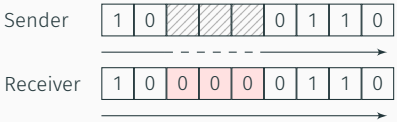

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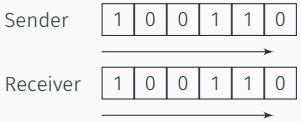

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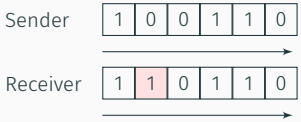

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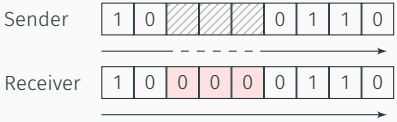

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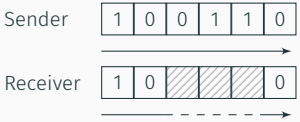

(d) Receiver descheduled: deletions

Our robust covert channel

- physical layer:
  - transmits words as a sequence of ‘0’s and ‘1’s
  - deals with synchronization errors
- data-link layer:
  - divides data to transmit into packets
  - corrects the remaining errors

C. Maurice et al. “Hello from the Other Side: SSH over Robust Cache Covert Channels in the Cloud”. In: *NDSS’17*. 2017

Physical layer: Sending ‘0’s and ‘1’s

- sender and receiver agree on one set

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- sender and receiver agree on one set
- receiver probes the set continuously
- sender transmits ’0’ doing nothing
  - → lines of the receiver still in cache → fast access
- sender transmits ’1’ accessing addresses in the set
  - → evicts lines of the receiver → slow access

Eviction set generation

- need a set of addresses in the same cache set and same slice

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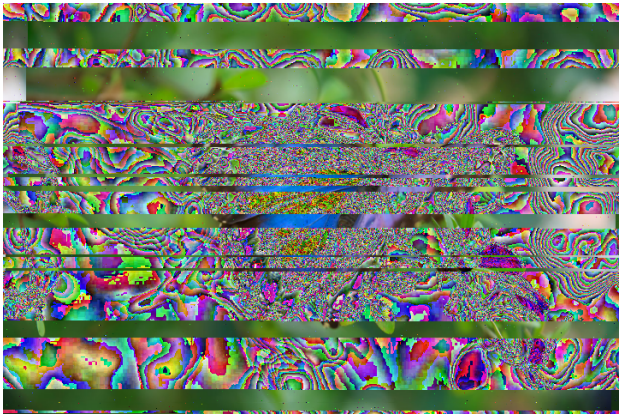
→ we use a jamming agreement

Sending the first image



Handling synchronization errors

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- deletion errors: request-to-send scheme that also serves as ack
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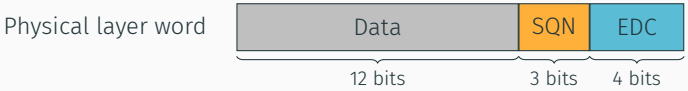
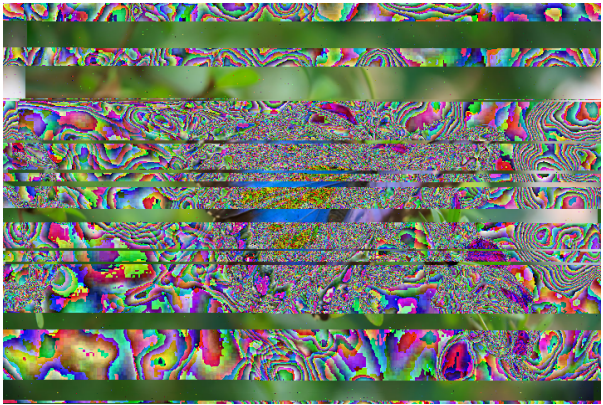
  - appending the number of '0's in the word to itself

  → property: a word cannot consist solely of '0's



Synchronization (before)



Synchronization (after)

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Data-link layer: Error correction

- Reed-Solomon codes to correct the remaining errors

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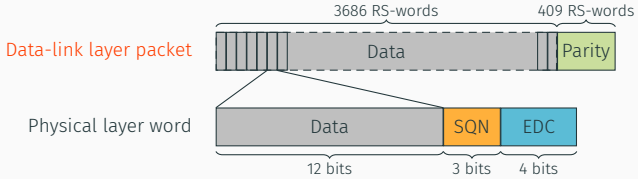
- Reed-Solomon codes to correct the remaining errors
- RS word size = physical layer word size = 12 bits
- packet size = $2^{12} - 1 = 4095$ RS words
- 10% error-correcting code: 409 parity and 3686 data RS words



Error correction (after)

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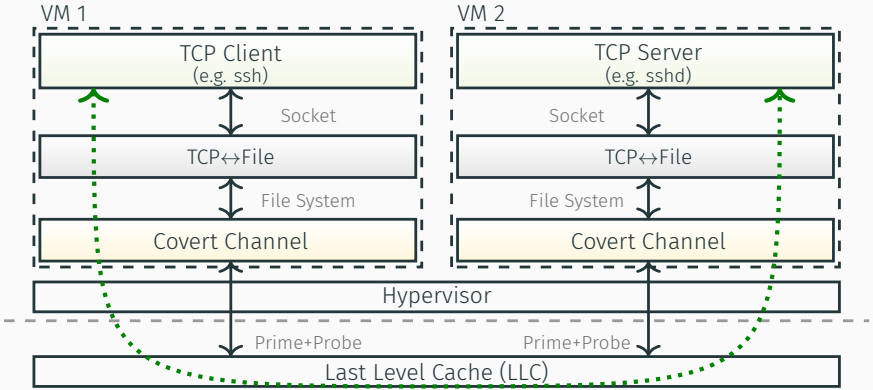
Amazon EC2	45.09 KBps	0.00%	web server serving files on sender VM
Amazon EC2	42.96 KBps	0.00%	`stress -m 2` on sender VM
Amazon EC2	42.26 KBps	0.00%	`stress -m 1` on receiver VM
Amazon EC2	37.42 KBps	0.00%	web server on all 3 VMs, `stress -m 4` on 3rd VM, `stress -m 1` on sender and receiver VMs
Amazon EC2	34.27 KBps	0.00%	`stress -m 8` on third VM

Building an SSH connection



SSH evaluation

Between two instances on Amazon EC2

Noise	Connection
No noise	✓
`stress -m 8` on third VM	✓
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Telnet also works with occasional corrupted bytes with `stress -m 1`

Countermeasures

Countermeasures

- different levels: hardware, system, application
- different goals
  - remove interferences
  - add noise to interferences
  - make it impossible to measure interferences

Hardware level: Fixing the instruction set?

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→ require changes to the architecture

→ there are other sources of timing

→ attacks still possible (e.g., Prime+Probe)

Hardware level: Stop sharing hardware?

- stop sharing cache

G. Irazoqui et al. “Cross processor cache attacks”. In: *AsiaCCS’16*. 2016

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Hardware level: Stop sharing hardware?

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- not an option for cost reasons in the cloud

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- stop sharing cache → attacks are getting better
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  - current attacks on LLC → across cores → stop sharing CPU
  - 2016: first attack across processors → what next?
- not an option for cost reasons in the cloud
- what about JavaScript attacks?

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Hardware level: Changes in microarchitecture

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→ performance and cost win, no implementation by manufacturers

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System level: Prevention

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- noise in timers or no timer
  - → adding noise makes attacks harder, not impossible
  - → removing timers is not realistic

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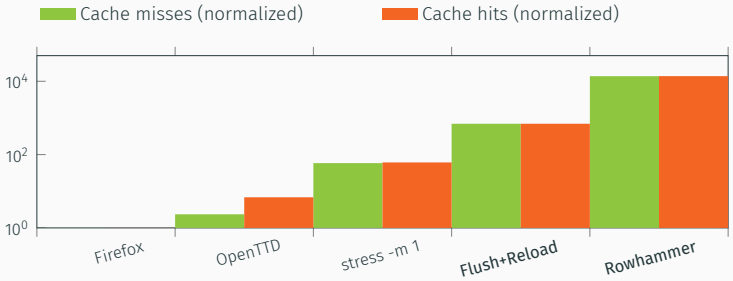
System level: Detect on-going attacks

- using performance counters to monitor cache hits and cache misses

→ risk of false positives



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Application level: Detect leakage

- CacheAudit : static analysis of source code
- Cache Template Attacks : dynamic approach

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Application level: Detect leakage

- CacheAudit : static analysis of source code
- Cache Template Attacks : dynamic approach

→ limited to side-channels → covert channels still possible

→ most effective for critical code

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Application level: Write better code

- no branch or data access depending on a secret
- hardware implementations (AES-NI, etc.)

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- no branch or data access depending on a secret
- hardware implementations (AES-NI, etc.)

→ protecting crypto is possible and necessary!

→ a few CVEs that have been treated: CVE-2005-0109, CVE-2013-4242, CVE-2014-0076, CVE-2016-0702, CVE-2016-2178, CVE-2016-7440, CVE-2016-7439, CVE-2016-7438, CVE-2018-0737, ...

Bigger perspective and conclusions

`rdseed` and floating point operations

- `rdseed`
  - request a random seed to the hardware random number generator
  - fixed number of precomputed random bits, takes time to regenerate them

  $\rightarrow$ covert channel

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- `rdseed`
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  → covert channel
- `fadd`, `fmul`
  - floating-point unit
  - floating point operations running time depends on the operands

  → bypassing Firefox's same origin policy via SVG filter timing attack

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`jmp` and TSX instructions

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  → covert channels, side-channel attacks on crypto, bypassing kernel ASLR

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`jmp` and TSX instructions

- `jmp`
  - branch prediction and branch target prediction → branch prediction unit

  → covert channels, side-channel attacks on crypto, bypassing kernel ASLR
- TSX instructions
  - extension for transactional memory support in hardware

  → bypassing kernel ASLR

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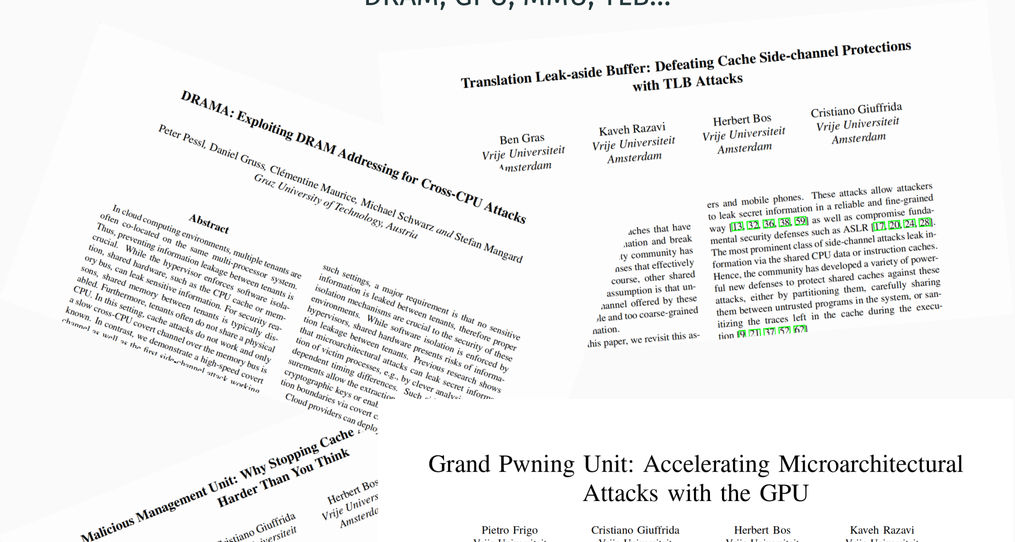
It’s not just caches!

DRAM, GPU, MMU, TLB...



DRAMA: Exploiting DRAM Addressing for Cross-CPU Attacks

Peter Pessl, Daniel Gruss, Clémentine Maurice, Michael Schwarz *and* Stefan Mangard
Graz University of Technology, Austria

Translation Leak-aside Buffer: Defeating Cache Side-channel Protections with TLB Attacks

Ben Gras, *Vrije Universiteit Amsterdam*; Kaveh Razavi, *Vrije Universiteit Amsterdam*; Herbert Bos, *Vrije Universiteit Amsterdam*; Cristiano Giuffrida, *Vrije Universiteit Amsterdam*

Malicious Management Unit: Why Stopping Cache Attacks in Software is Harder Than You Think

Grand Pwning Unit: Accelerating Microarchitectural Attacks with the GPU

Pietro Frigo, Cristiano Giuffrida, Herbert Bos, Kaveh Razavi

Conclusion

- more a problem of CPU design than Instruction Set Architecture

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Conclusion

- more a problem of CPU design than Instruction Set Architecture
- it's also not just the cache
- hard to patch $\rightarrow$ issues linked to performance optimizations
- we would like to keep the optimizations without the attacks
- very interesting and active field of research!

Questions?

Contact

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Introduction to cache side-channel attacks

Clémentine Maurice, CNRS, IRISA

October 9, 2018—Séminaire du DIT, ENS Rennes

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