Cache attacks:
Software side-channel and fault attacks

Clémentine Maurice, Graz University of Technology

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Who am I

- Clémentine Maurice
- PhD in computer science, Postdoc @ Graz University Of Technology
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+ Secure Systems team: Daniel Gruss, Michael Schwarz, Moritz Lipp

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- remote side-channel attacks

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→ crypto and sensitive info., e.g., keystrokes and mouse movements

Sources of leakage

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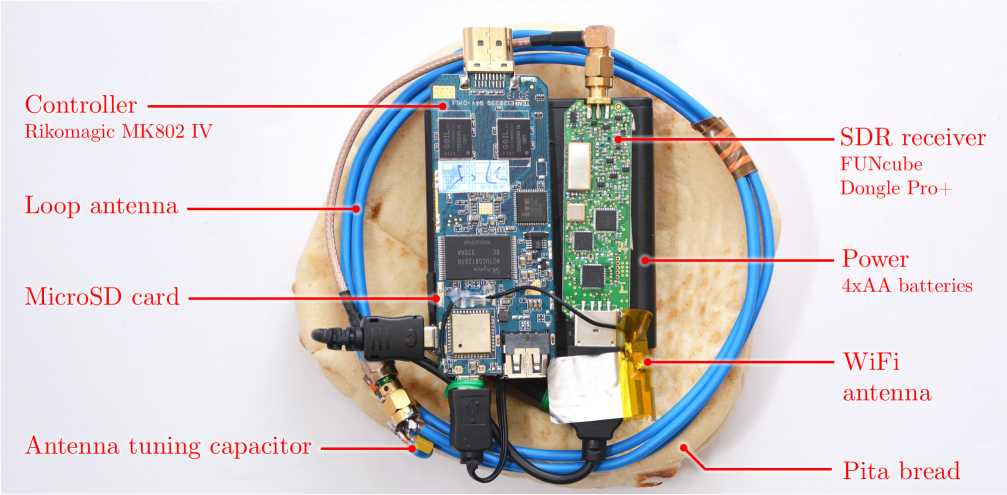

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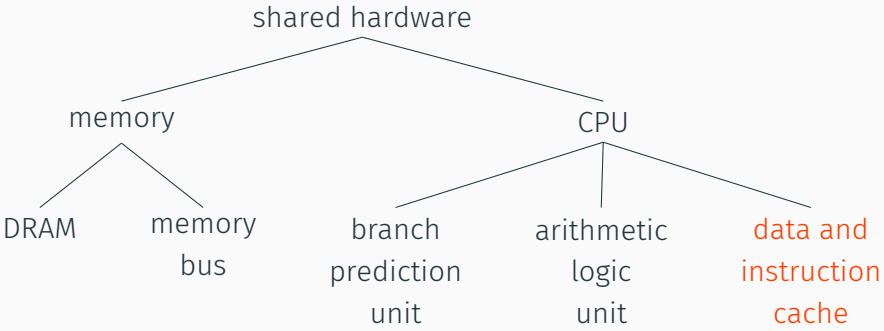
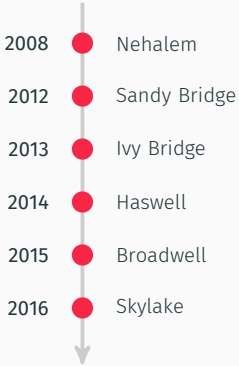
  - → remote attacks

Shared hardware



From small optimizations to side channels



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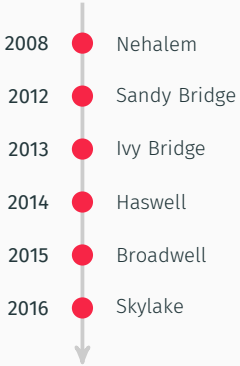

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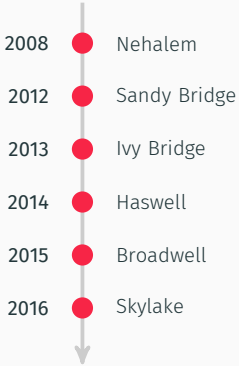

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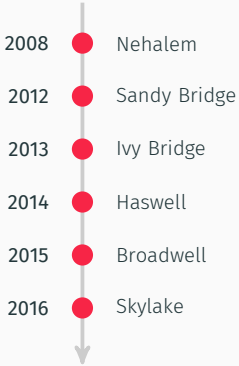

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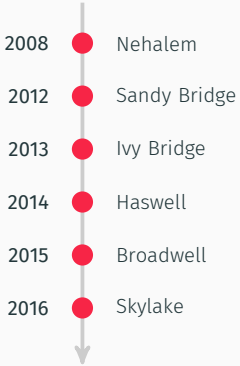

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- no documentation on this intellectual property

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Outline

- Background
- Cache covert channels
- Side-channel attacks on crypto, keystrokes, and KASLR
- Fault attacks on DRAM in JavaScript
- Countermeasures and conclusion

Cache Attack Techniques

MOV—Move

Opcode	Instruction	Op/ En	64-Bit Mode	Compat/ Leg Mode	Description
88 /r	MOV *r/m8,r8*	MR	Valid	Valid	Move *r8* to *r/m8*.
REX + 88 /r	MOV *r/m8****,*r8****	MR	Valid	N.E.	Move *r8* to *r/m8*.
89 /r	MOV *r/m16,r16*	MR	Valid	Valid	Move *r16* to *r/m16*.
89 /r	MOV *r/m32,r32*	MR	Valid	Valid	Move *r32* to *r/m32*.
REX.W + 89 /r	MOV *r/m64,r64*	MR	Valid	N.E.	Move *r64* to *r/m64*.
8A /r	MOV *r8,r/m8*	RM	Valid	Valid	Move *r/m8* to *r8*.
REX + 8A /r	MOV *r8****,*r/m8****	RM	Valid	N.E.	Move *r/m8* to *r8*.
8B /r	MOV *r16,r/m16*	RM	Valid	Valid	Move *r/m16* to *r16*.
8B /r	MOV *r32,r/m32*	RM	Valid	Valid	Move *r/m32* to *r32*.
REX.W + 8B /r	MOV *r64,r/m64*	RM	Valid	N.E.	Move *r/m64* to *r64*.
8C /r	MOV *r/m16,Sreg***	MR	Valid	Valid	Move segment register to *r/m16*.
REX.W + 8C /r	MOV *r/m64,Sreg***	MR	Valid	Valid	Move zero extended 16-bit segment register to *r/m64*.
8E /r	MOV *Sreg,r/m16***	RM	Valid	Valid	Move *r/m16* to segment register.
REX.W + 8E /r	MOV *Sreg,r/m64***	RM	Valid	Valid	Move *lower 16 bits of r/m64* to segment register.
A0	MOV AL,*moffs8**	FD	Valid	Valid	Move byte at (*seg:offset*) to AL.
REX.W + A0	MOV AL,*moffs8**	FD	Valid	N.E.	Move byte at (*offset*) to AL.
A1	MOV AX,*moffs16**	FD	Valid	Valid	Move word at (*seg:offset*) to AX.
A1	MOV EAX,*moffs32**	FD	Valid	Valid	Move doubleword at (*seg:offset*) to EAX.
REX.W + A1	MOV RAX,*moffs64**	FD	Valid	N.E.	Move quadword at (*offset*) to RAX.

mov

64-Bit Mode Exceptions

#GP(0)	If the memory address is in a non-canonical form.
	If an attempt is made to load SS register with NULL segment selector when CPL = 3.
	If an attempt is made to load SS register with NULL segment selector when CPL < 3 and CPL ≠ RPL.
#GP(selector)	If segment selector index is outside descriptor table limits.
	If the memory access to the descriptor table is non-canonical.
	If the SS register is being loaded and the segment selector's RPL and the segment descriptor's DPL are not equal to the CPL.
	If the SS register is being loaded and the segment pointed to is a nonwritable data segment.
	If the DS, ES, FS, or GS register is being loaded and the segment pointed to is not a data or readable code segment.
	If the DS, ES, FS, or GS register is being loaded and the segment pointed to is a data or nonconforming code segment, but both the RPL and the CPL are greater than the DPL.
#SS(0)	If the stack address is in a non-canonical form.
#SS(selector)	If the SS register is being loaded and the segment pointed to is marked not present.
#PF(fault-code)	If a page fault occurs.
#AC(0)	If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD	If attempt is made to load the CS register.
	If the LOCK prefix is used.

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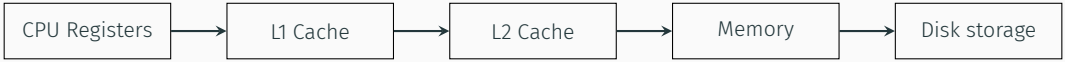
→ side effects on computations!

Memory hierarchy



- data can reside in

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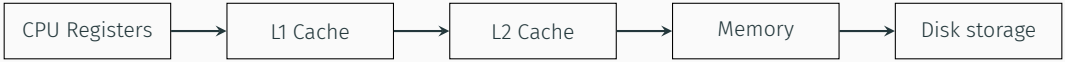

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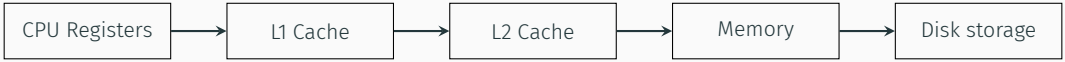

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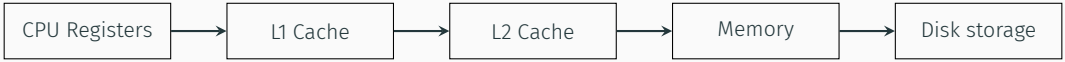

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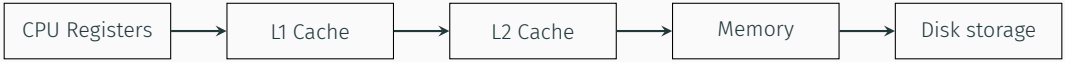

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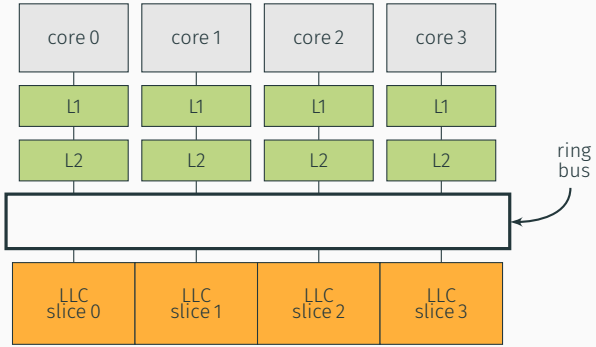

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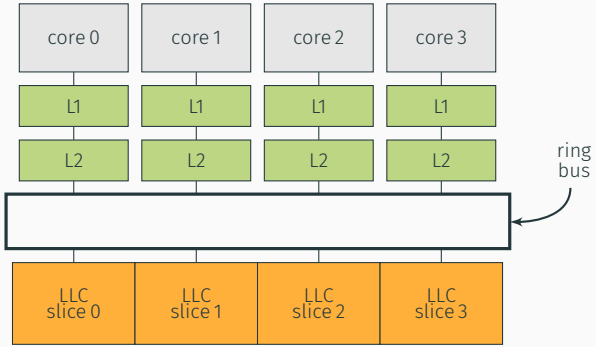

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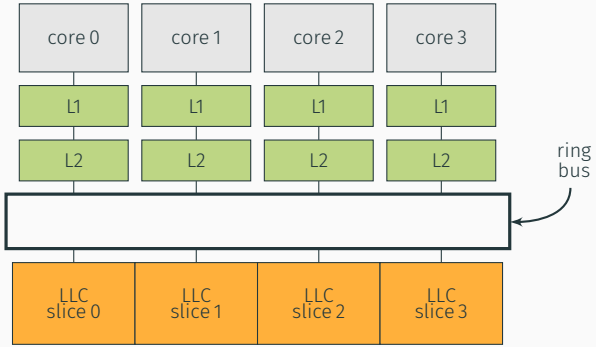

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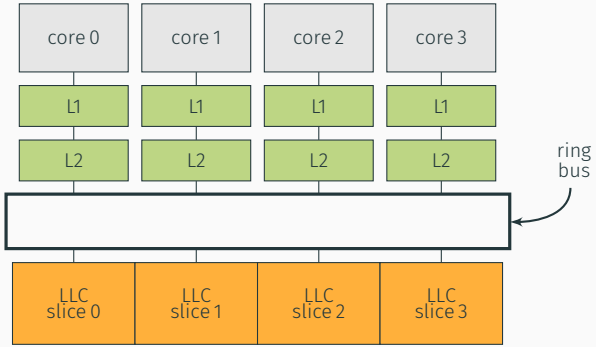

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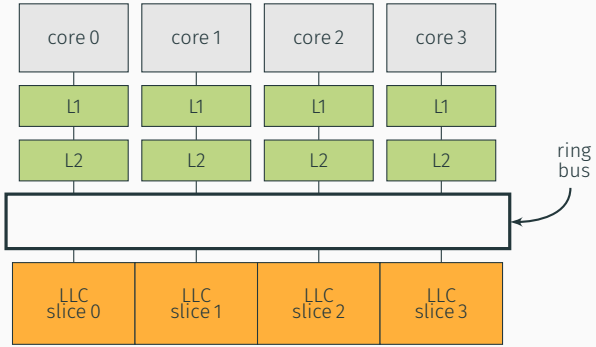

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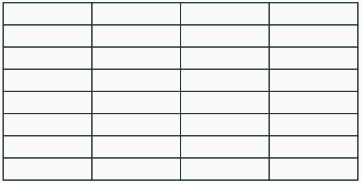

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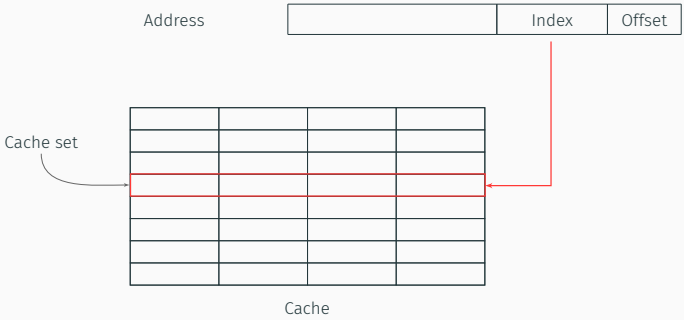

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Several ways per set

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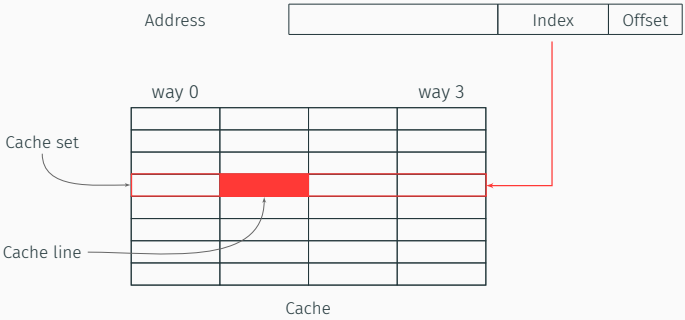
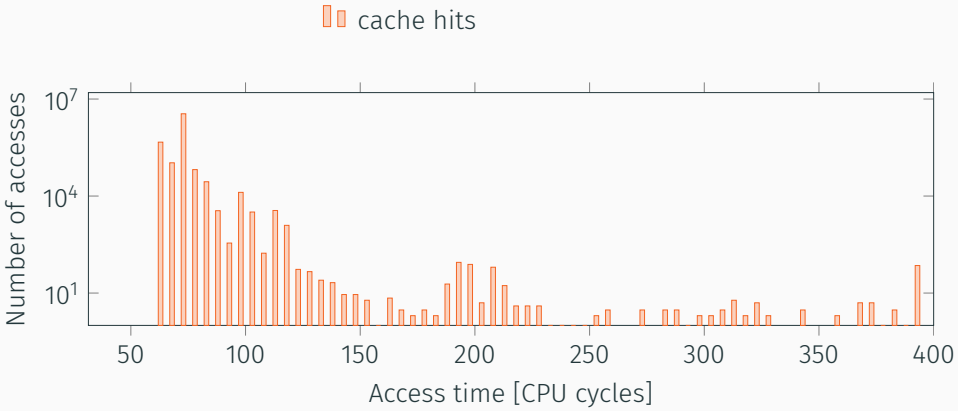


Data loaded in a specific set depending on its address

Several ways per set

Cache line loaded in a specific way depending on the replacement policy

Timing differences



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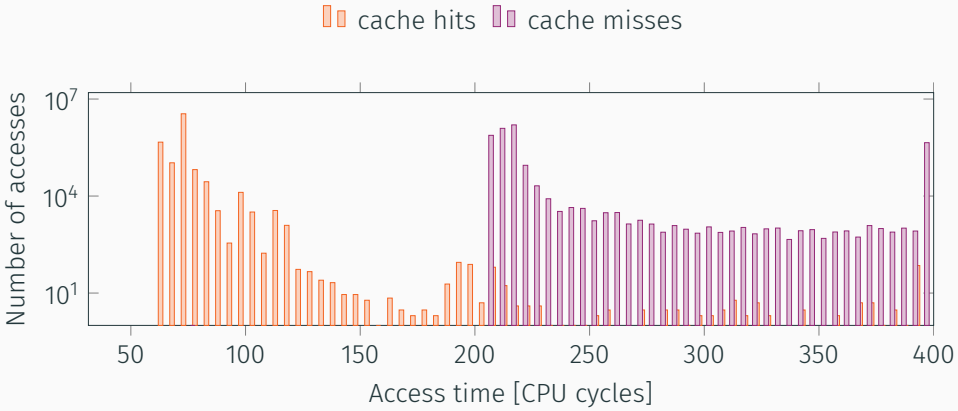

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[...]
rdtsc
function()
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[...]
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- do you measure what you think you measure?
- out-of-order execution → what is really executed

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Intel, *How to Benchmark Code Execution Times on Intel IA-32 and IA-64 Instruction Set Architectures White Paper*, December 2010.

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- attacker monitors which lines are accessed, not the content
- covert channel: two processes communicating with each other
  - not allowed to do so, e.g., across VMs
- side-channel attack: one malicious process spies on benign processes
  - e.g., steals crypto keys, spies on keystrokes

Cache attacks techniques

- two (main) techniques
  1. Flush+Reload (Gullasch et al., Osvik et al., Yarom et al.)
  2. Prime+Probe (Percival, Osvik et al., Liu et al.)
- exploitable on x86 and ARM

D. Gullasch et al. “Cache Games – Bringing Access-Based Cache Attacks on AES to Practice”. In: *S&P’11*. 2011.

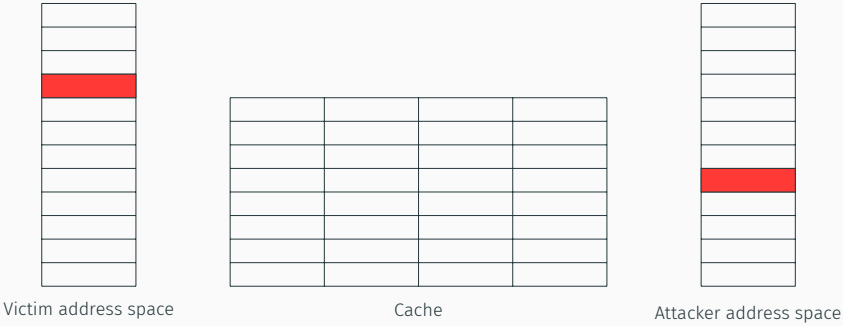
Y. Yarom et al. “Flush+Reload: a High Resolution, Low Noise, L3 Cache Side-Channel Attack”. In: *USENIX Security Symposium*. 2014.

D. A. Osvik et al. “Cache Attacks and Countermeasures: the Case of AES”. In: *CT-RSA 2006*. 2006.

C. Percival. “Cache missing for fun and profit”. In: *Proceedings of BSDCan*. 2005.

F. Liu et al. “Last-Level Cache Side-Channel Attacks are Practical”. In: *S&P’15*. 2015.

Cache attacks: Flush+Reload



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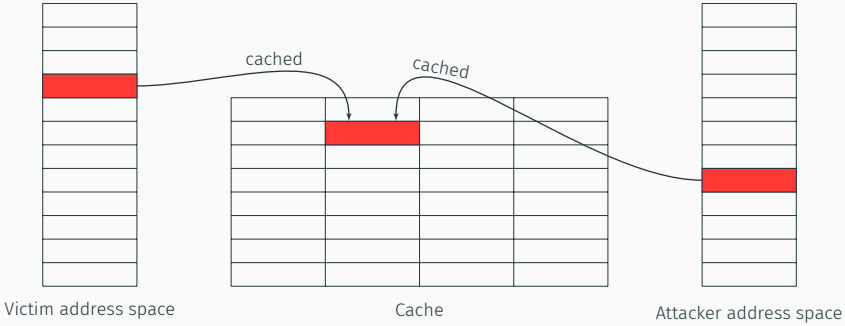

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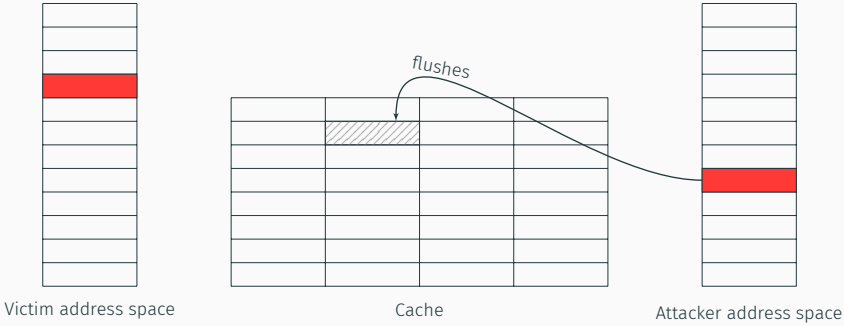

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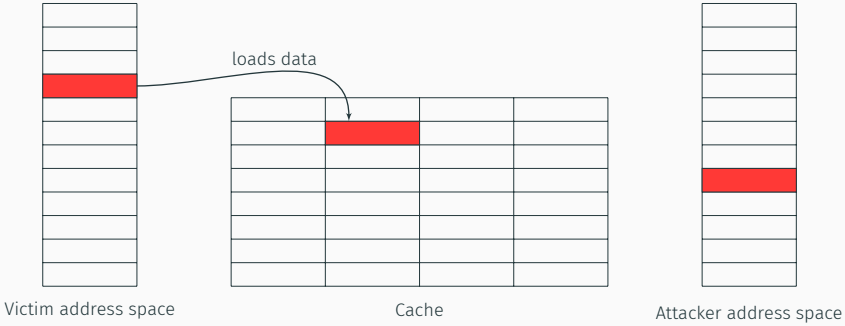
Step 2: Attacker flushes the shared cache line

Cache attacks: Flush+Reload



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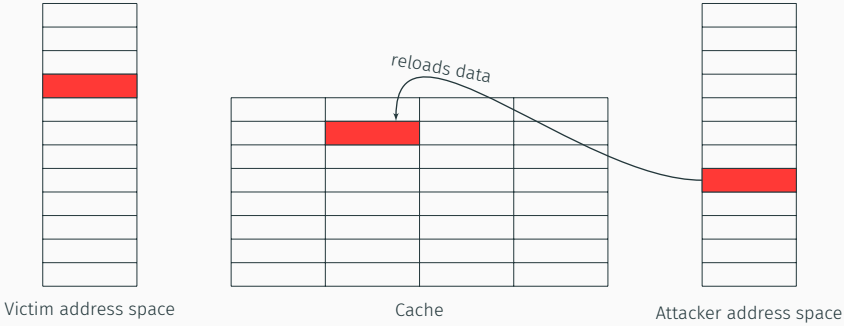

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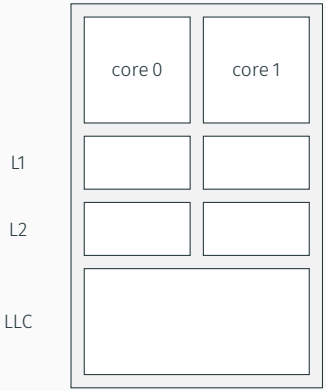
Step 4: Attacker reloads the data

What if there is no shared memory?

Inclusive property



- inclusive LLC: superset of L1 and L2

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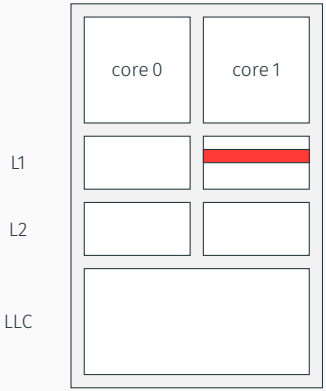

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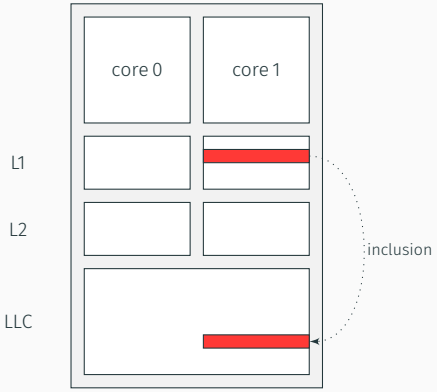

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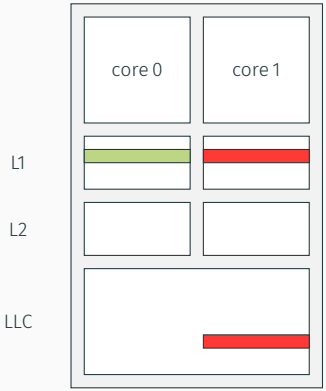

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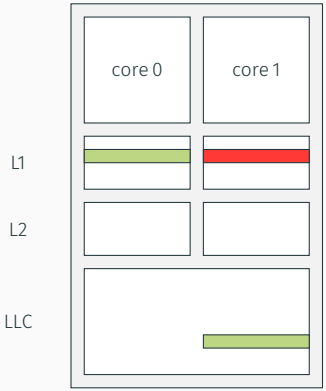

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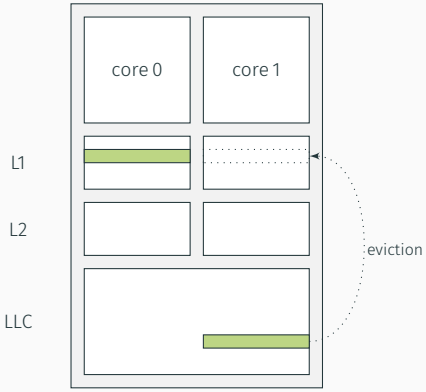

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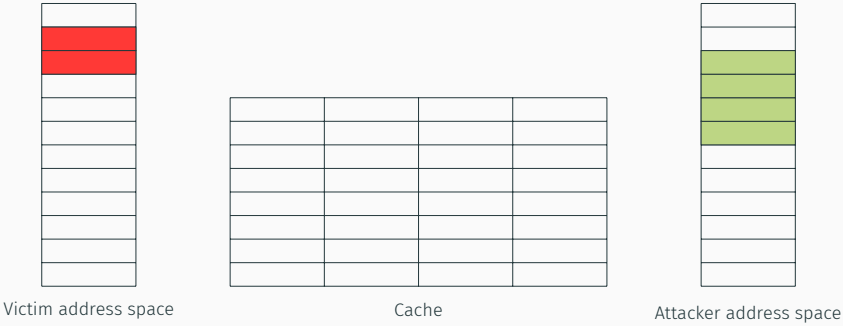

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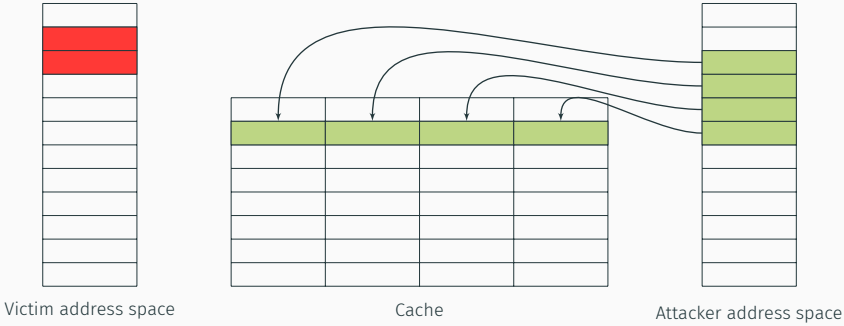

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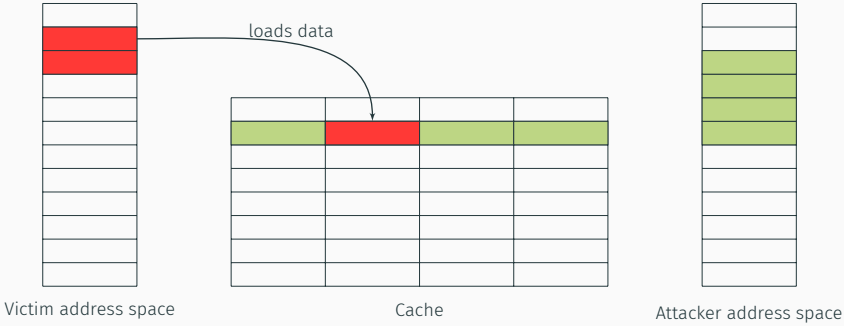

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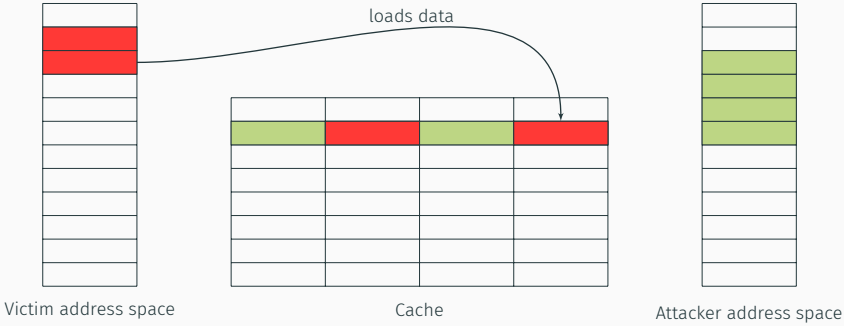

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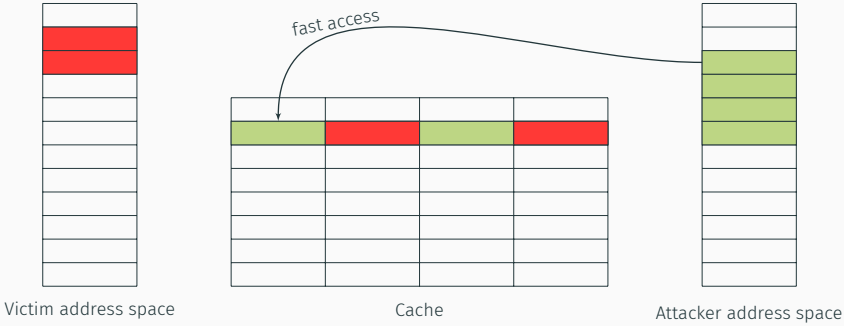

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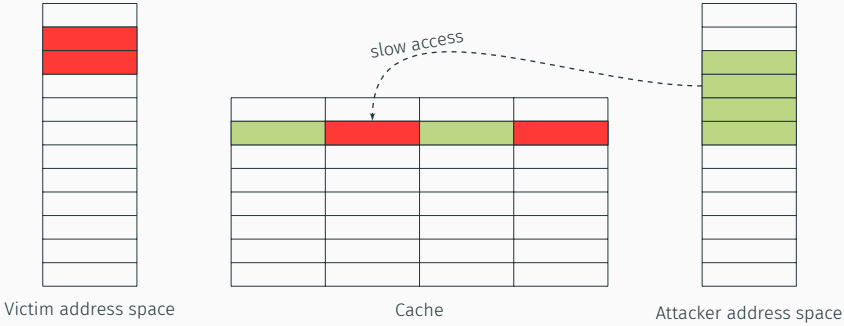

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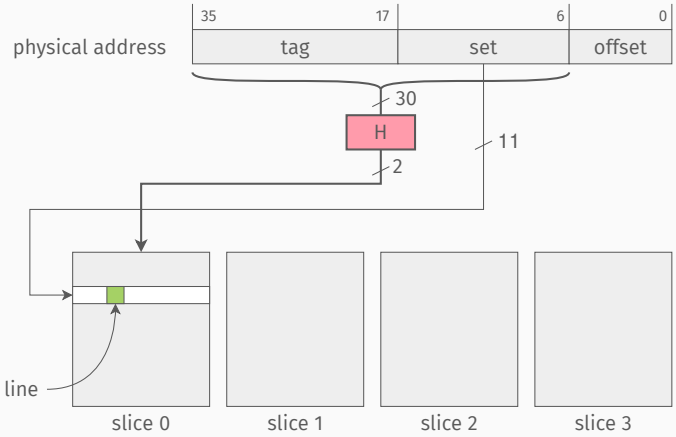
Last-level cache addressing



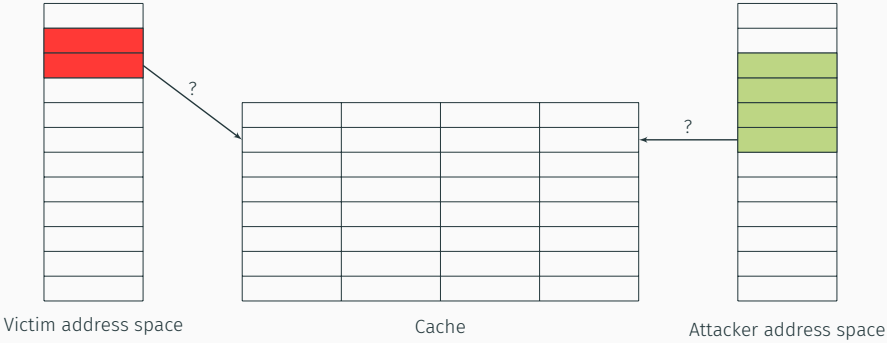
Last-level cache addressing

- last-level cache $\rightarrow$ as many slices as cores
- undocumented hash function that maps a physical address to a slice
- designed for performance

For 2^k slices:

Prime+Probe on recent procesors?

Undocumented function $\rightarrow$ impossible to target the same set in the same slice



Let’s reverse-engineer
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3. infer a function out of it

How to map addresses to slices?

- with performance counters (Maurice et al., 2015)
- with a timing attack
  - using `clflush` (using Gruss et al., 2016)
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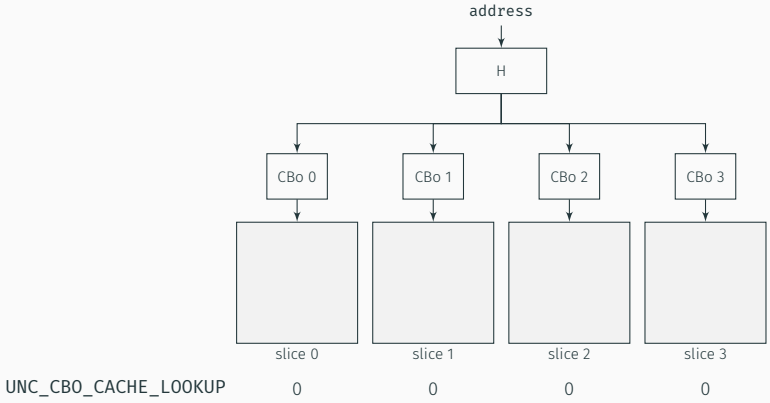

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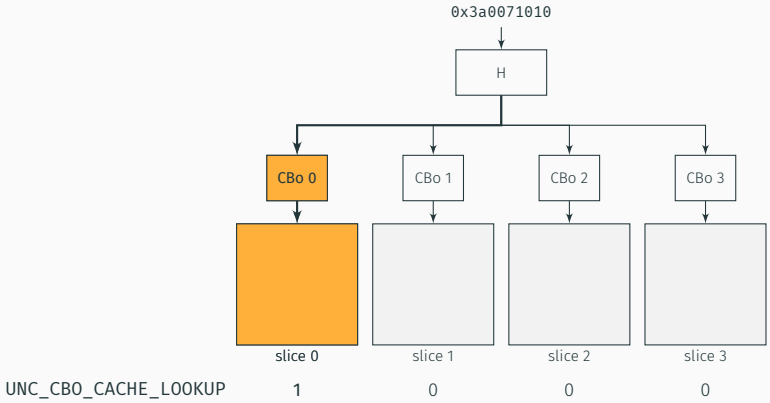

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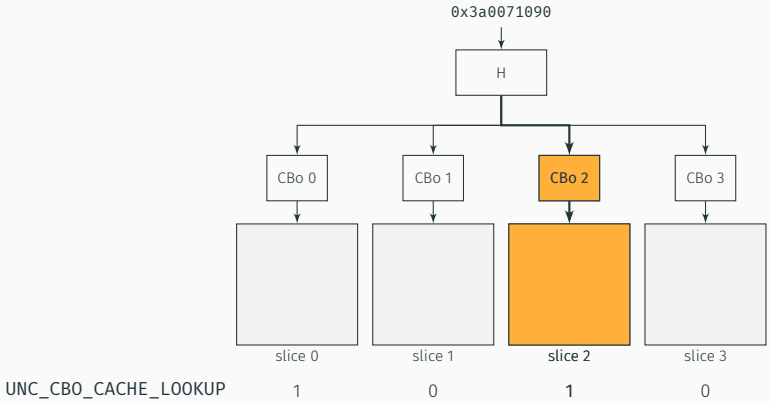

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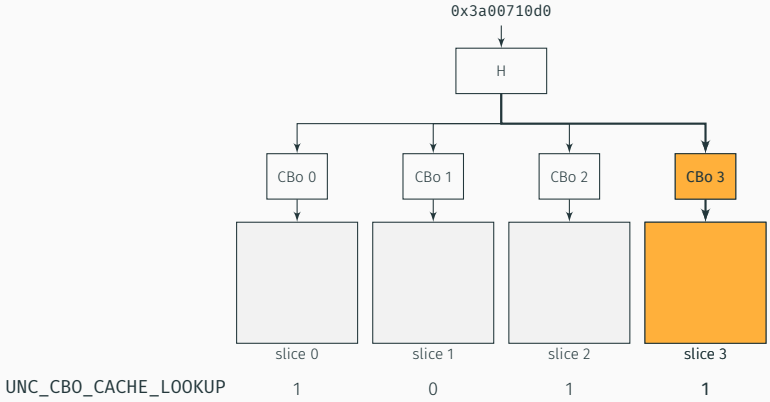

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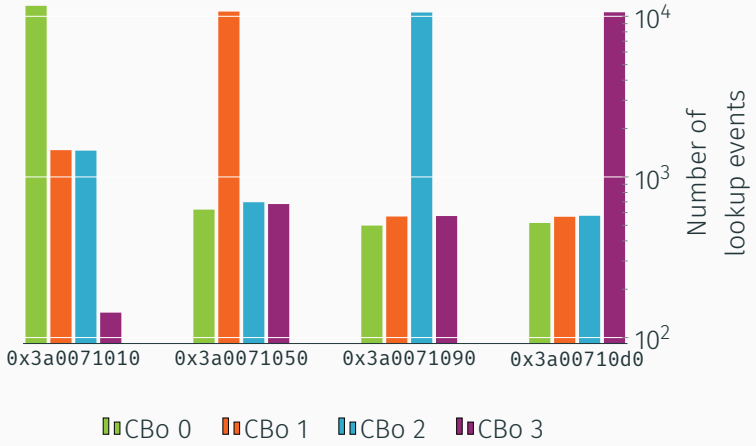

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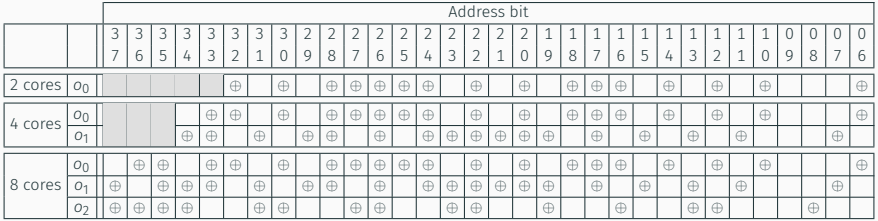
2. non-linear function (the rest): more complicated

Last-level cache linear functions

3 functions, depending on the number of cores



Function valid for Sandy Bridge, Ivy Bridge, Haswell, Broadwell

#1. Cache Covert Channels

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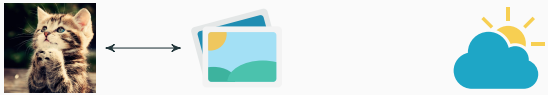

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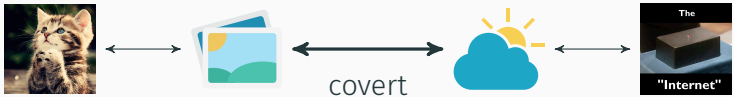

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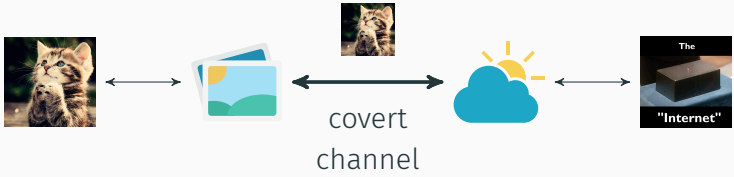

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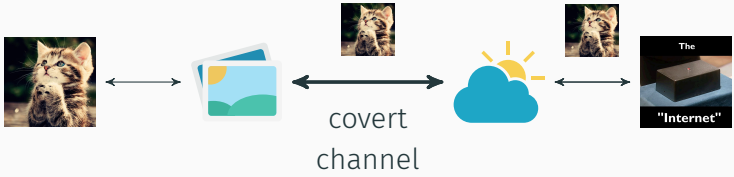

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- Prime+Probe: agreeing on a cache set
  - sender: primes the set to send '1', stays idle to send '0'
  - receiver: probes the set

Issues

- programs competing for
  - the CPU cache
  - scheduling

C. Maurice et al. “Hello from the Other Side: SSH over Robust Cache Covert Channels in the Cloud”. In: *NDSS’17*. 2017.

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- let’s investigate this!

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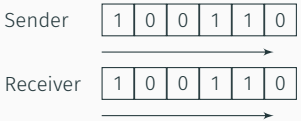
Why can’t we just use error correcting codes?



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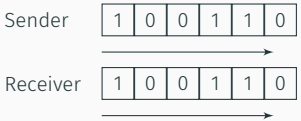

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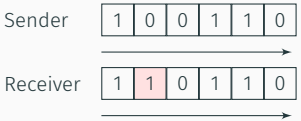

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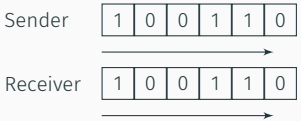

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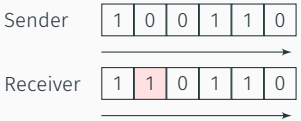

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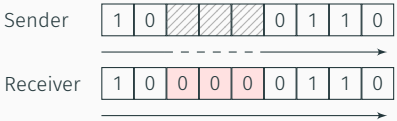

(c) Sender descheduled: insertions

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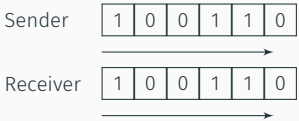
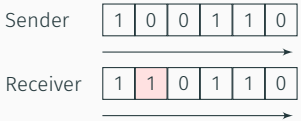
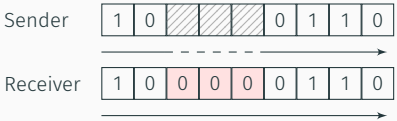


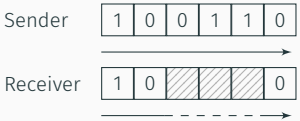
(a) Transmission without errors



(b) Noise: substitution error



(c) Sender descheduled: insertions



(d) Receiver descheduled: deletions

Our robust covert channel

- physical layer:
  - transmits words as a sequence of ‘0’s and ‘1’s
  - deals with synchronization errors
- data-link layer:
  - divides data to transmit into packets
  - corrects the remaining errors

Physical layer: Sending ‘0’s and ‘1’s

- sender and receiver agree on one set

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- sender and receiver agree on one set
- receiver probes the set continuously

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- sender and receiver agree on one set
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- sender transmits ’0’ doing nothing
  → lines of the receiver still in cache → fast access

Physical layer: Sending ‘0’s and ‘1’s

- sender and receiver agree on one set
- receiver probes the set continuously
- sender transmits ’0’ doing nothing
  → lines of the receiver still in cache → fast access
- sender transmits ’1’ accessing addresses in the set
  → evicts lines of the receiver → slow access

Eviction set generation

- need a set of addresses in the same cache set and same slice

Eviction set generation

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- problem: slice number depends on all bits of the physical address

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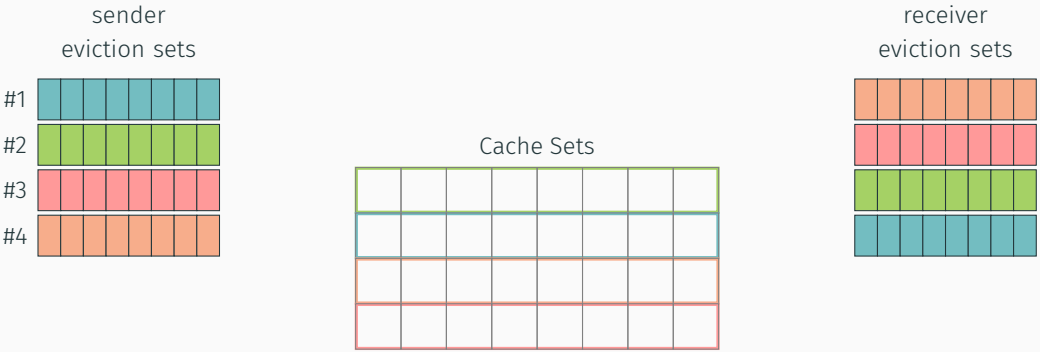
Eviction set generation

- need a set of addresses in the same cache set and same slice
- problem: slice number depends on all bits of the physical address

- we can build a set of addresses in the same cache set and same slice
- without knowing which slice

Jamming agreement



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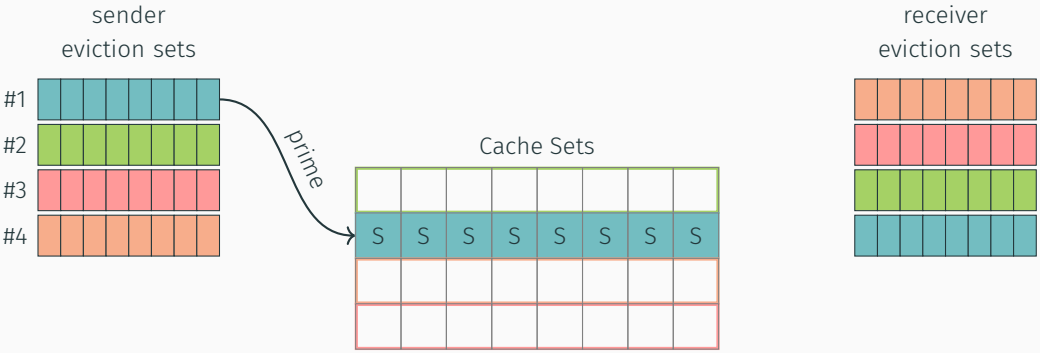

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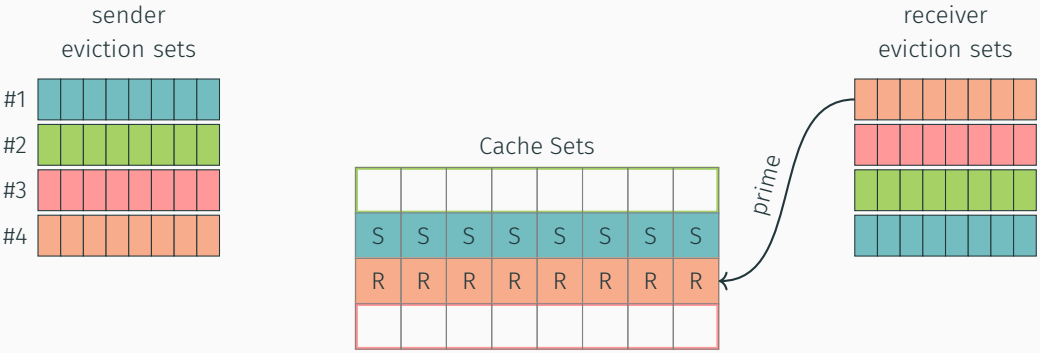

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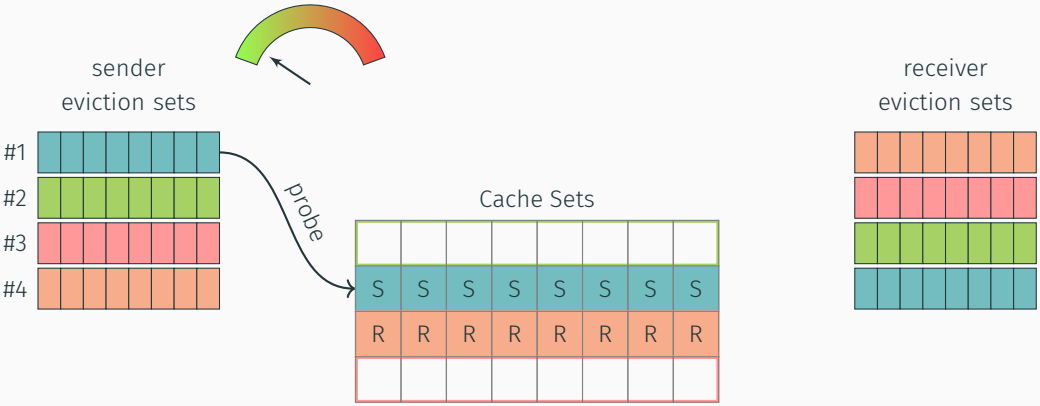

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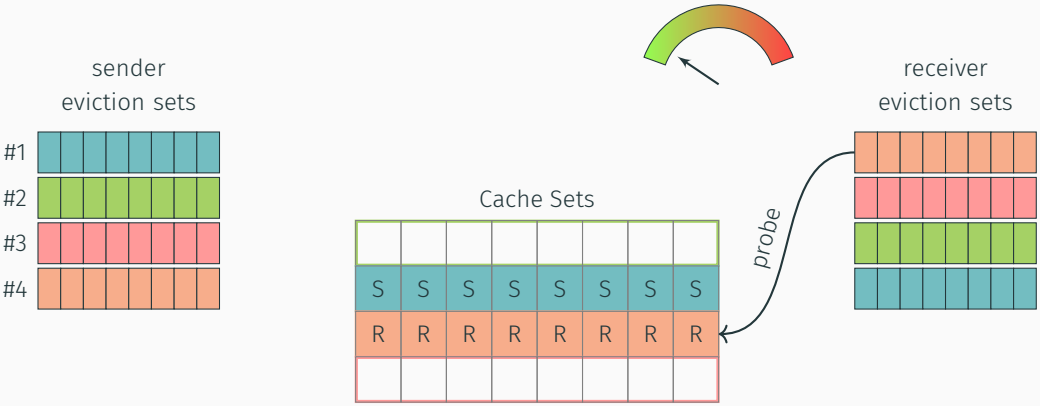
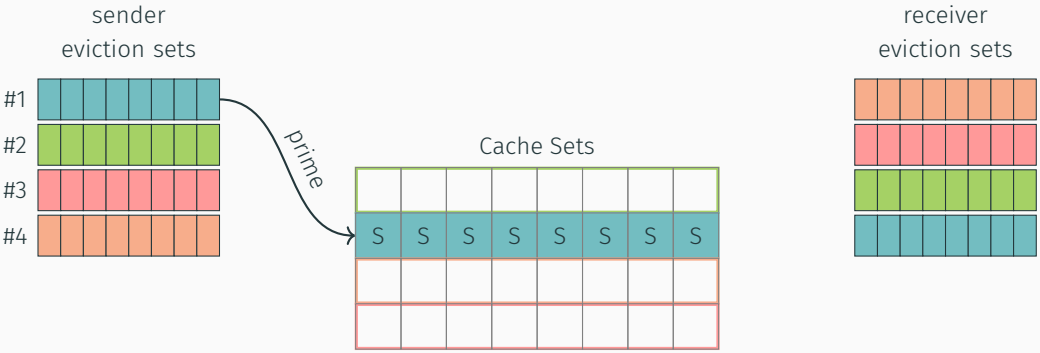
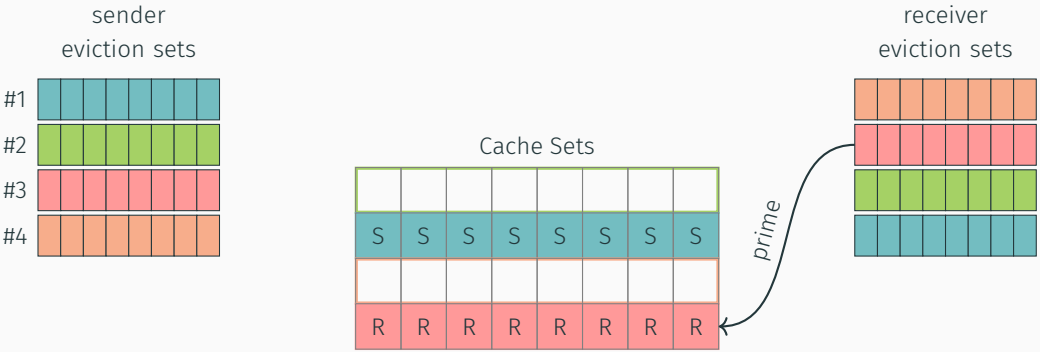


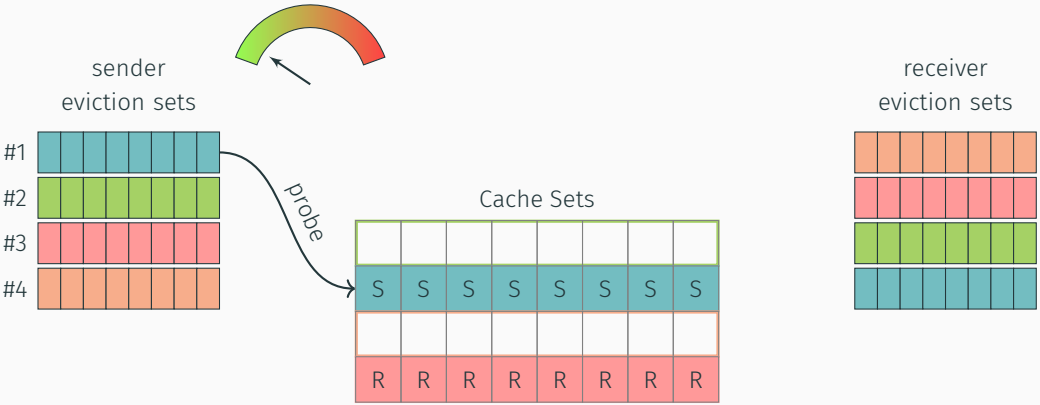
Jamming agreement



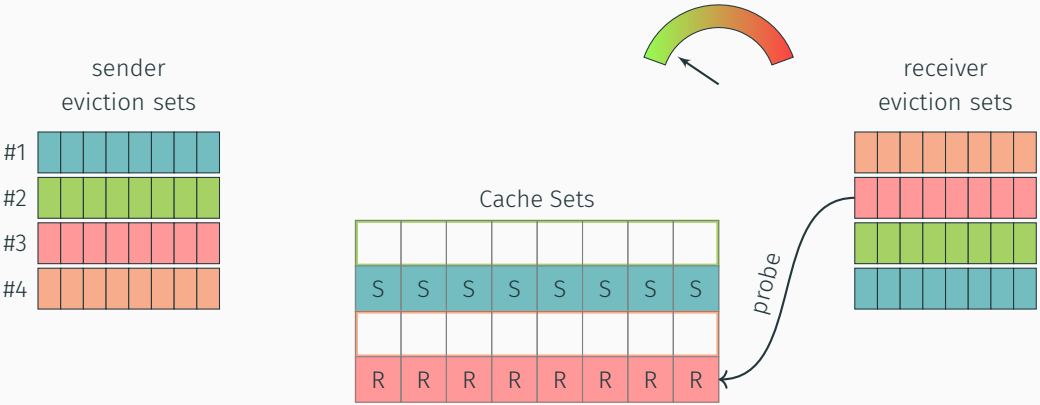
Jamming agreement



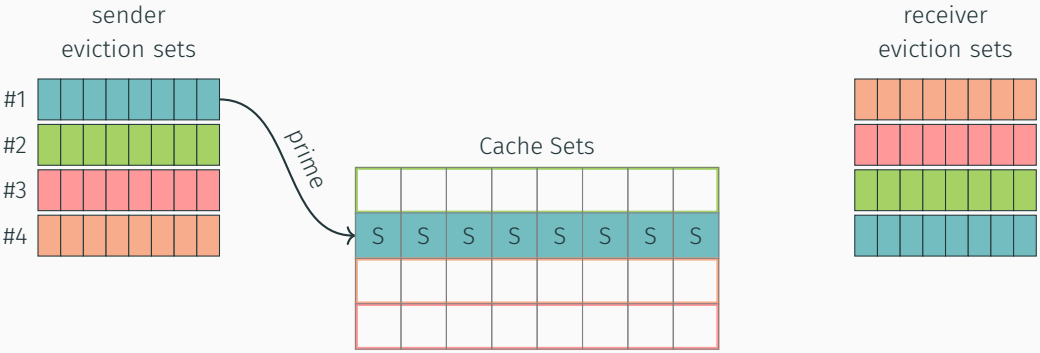
Jamming agreement



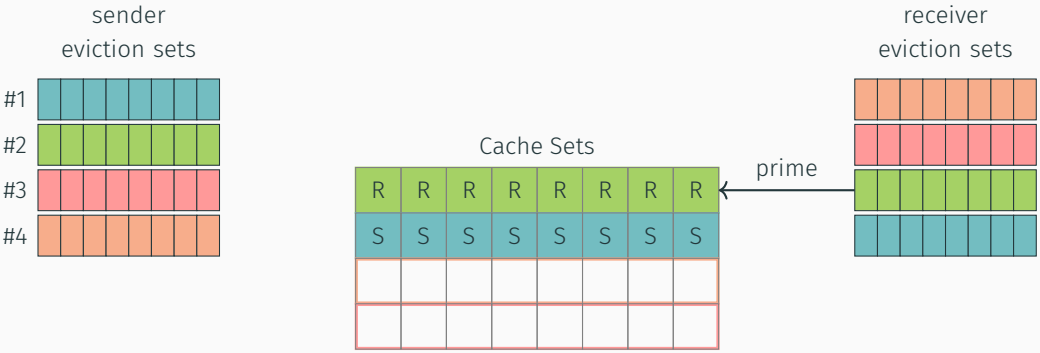
Jamming agreement



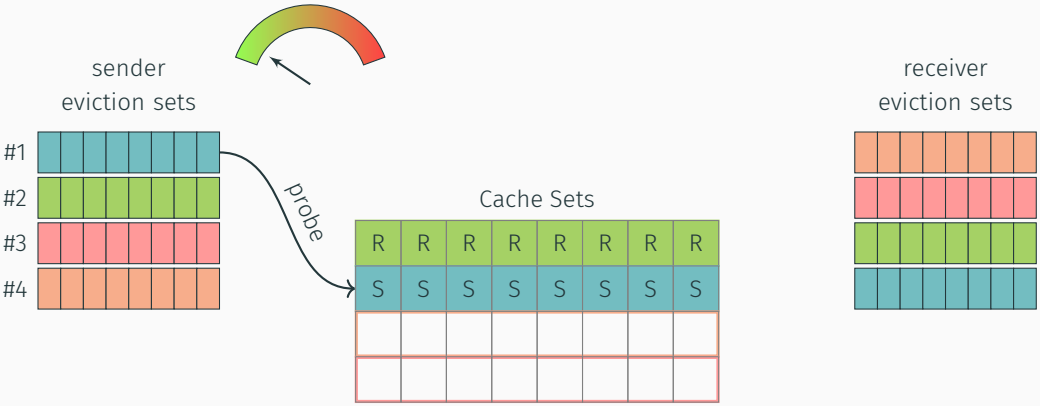
Jamming agreement



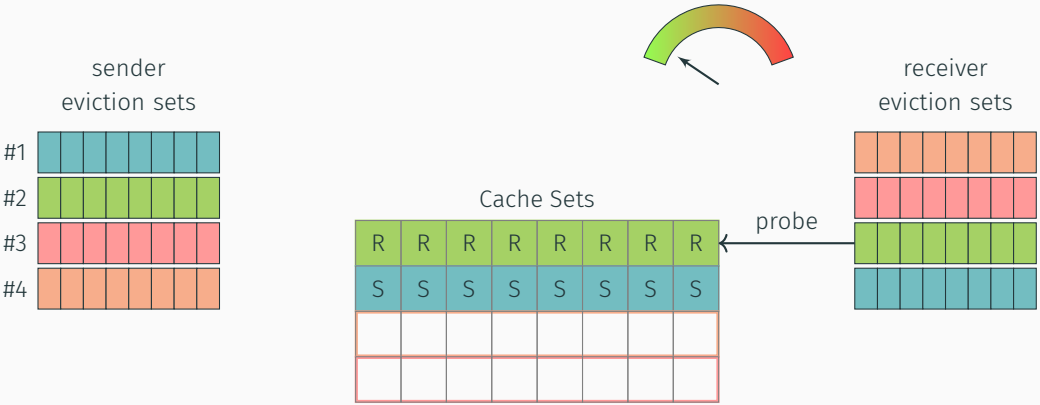
Jamming agreement



Jamming agreement



Jamming agreement



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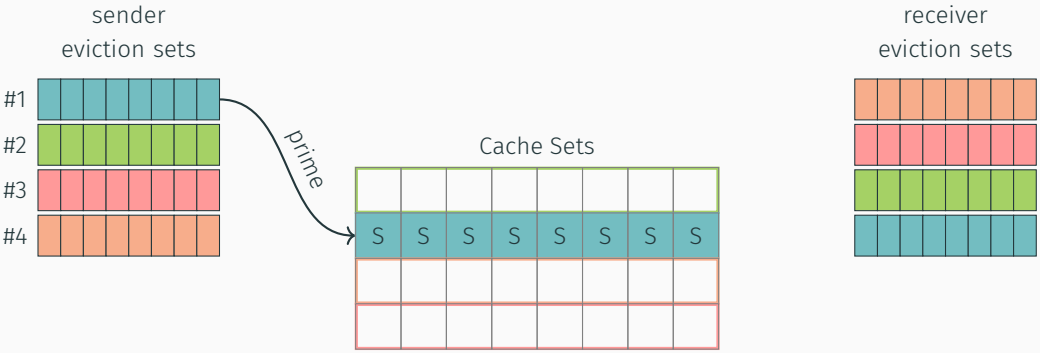

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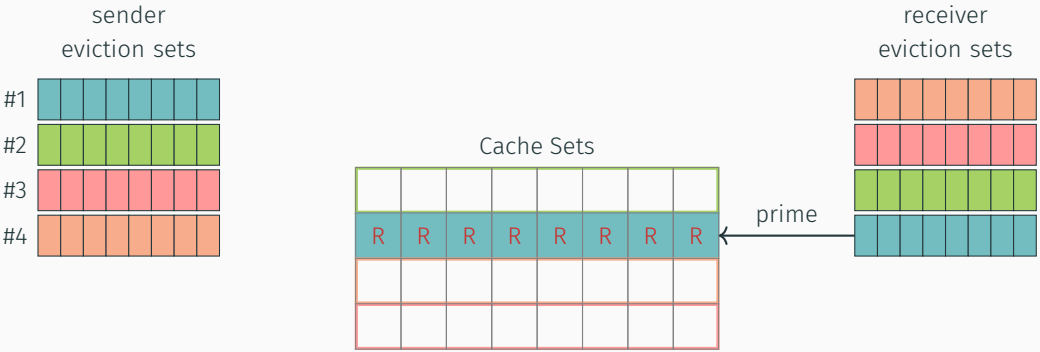

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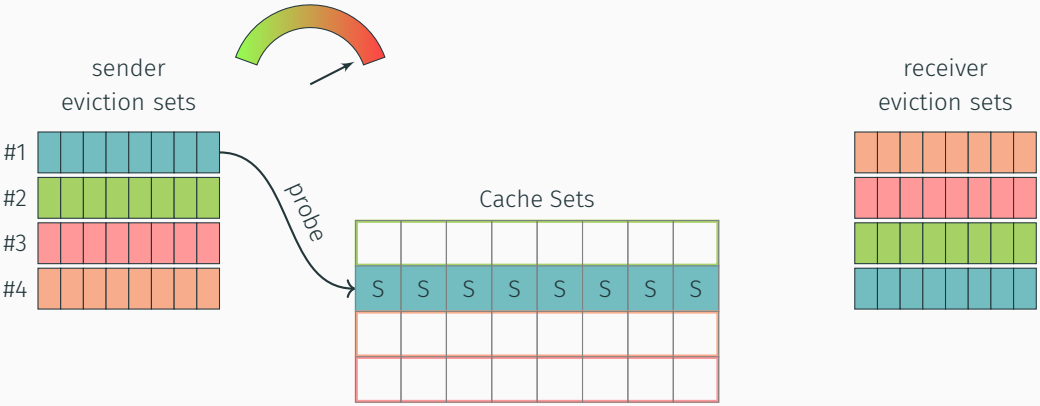
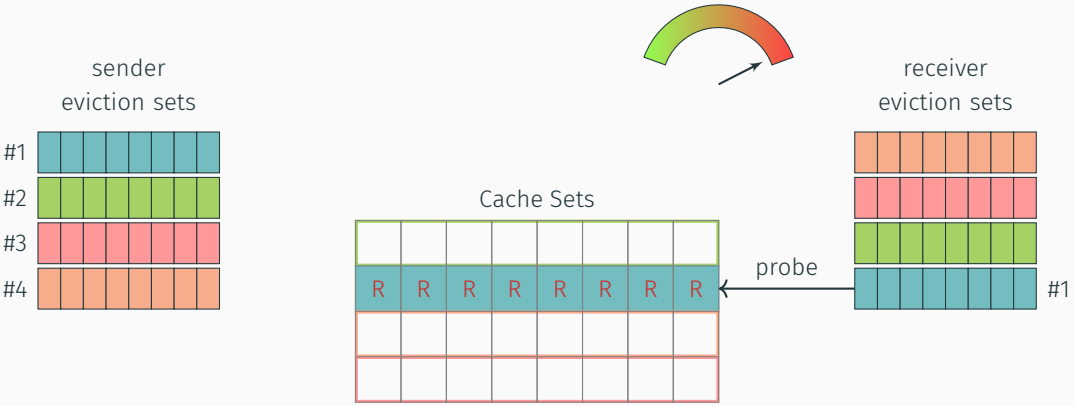


Jamming agreement



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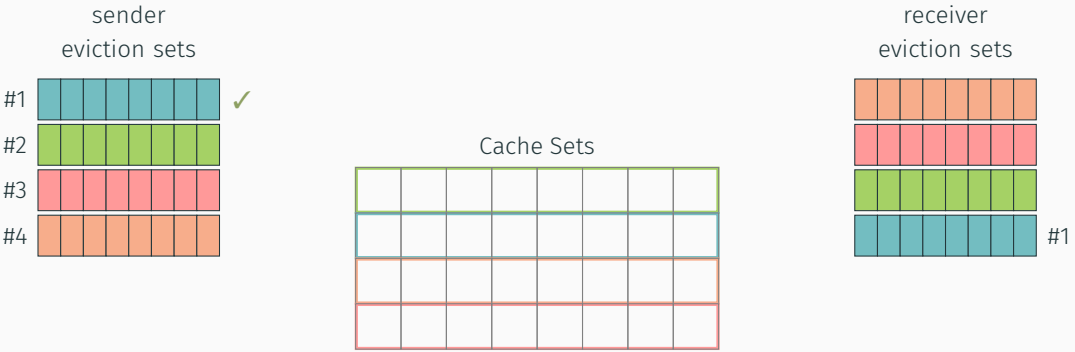
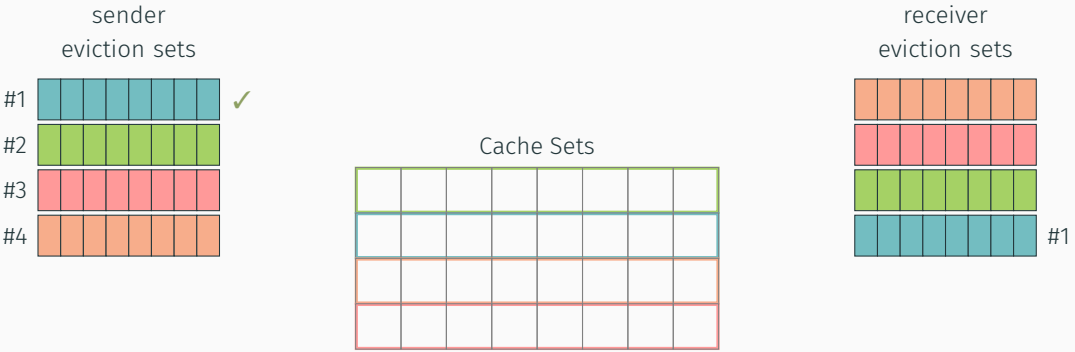


Jamming agreement



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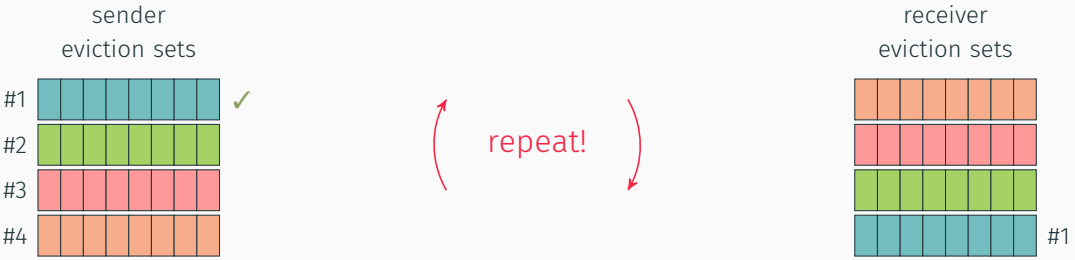

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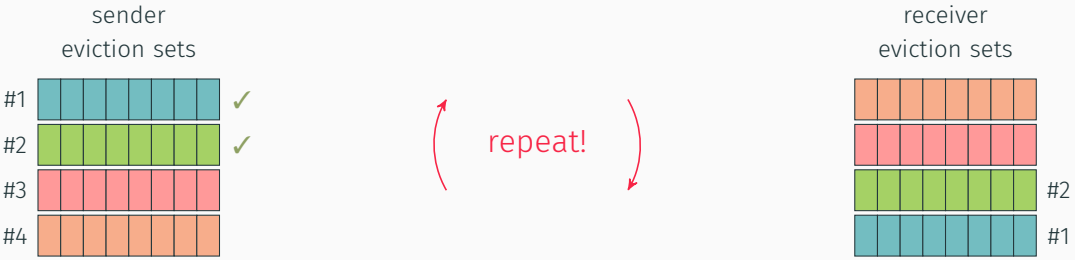
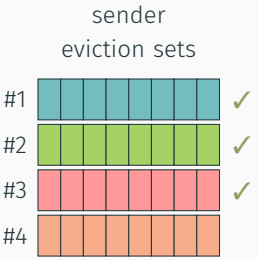
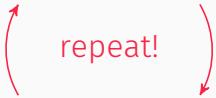
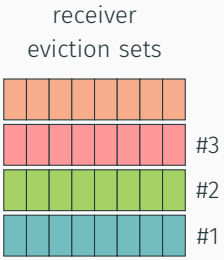


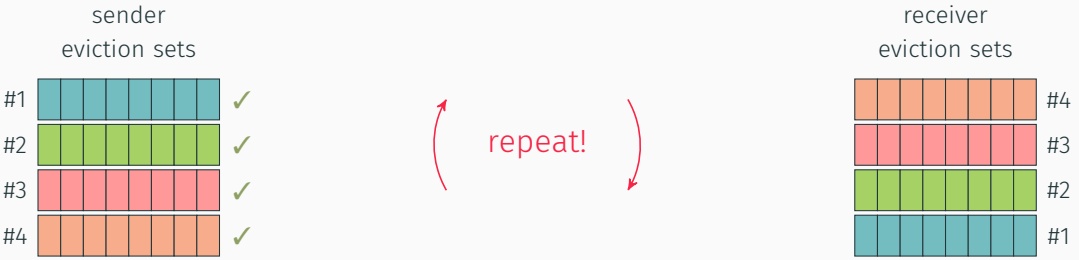
Jamming agreement



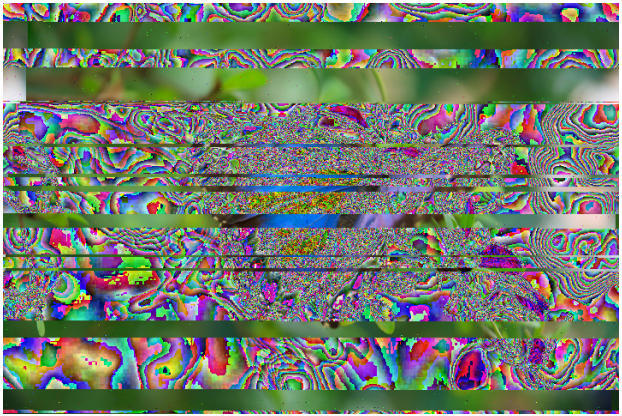




Jamming agreement



Sending the first image



Handling synchronization errors

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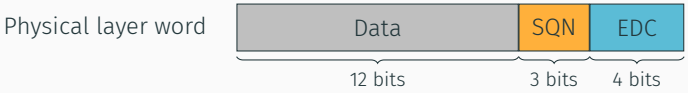
- deletion errors: request-to-send scheme that also serves as ack
  - 3-bit sequence number
  - request: encoded sequence number (7 bits)

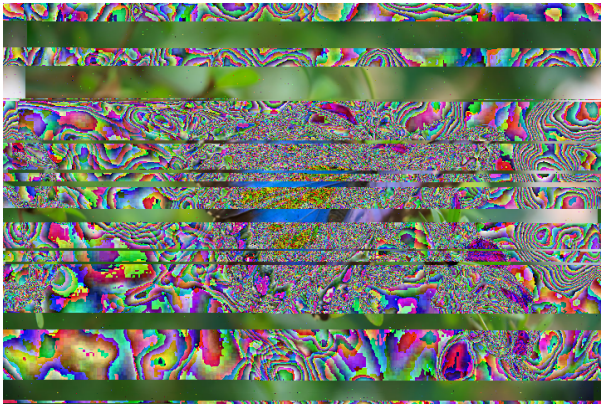
Handling synchronization errors

- deletion errors: request-to-send scheme that also serves as ack
  - 3-bit sequence number
  - request: encoded sequence number (7 bits)
- '0'-insertion errors: error detection code → Berger codes
  - appending the number of '0's in the word to itself

  → property: a word cannot consist solely of '0's



Synchronization (before)



Synchronization (after)

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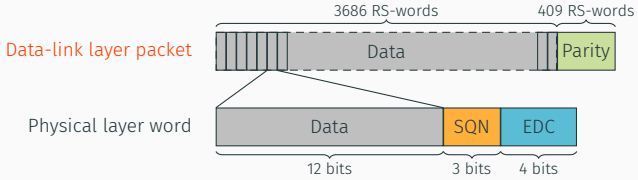
Synchronization (after)

Data-link layer: Error correction

- Reed-Solomon codes to correct the remaining errors

Data-link layer: Error correction

- Reed-Solomon codes to correct the remaining errors
- RS word size = physical layer word size = 12 bits
- packet size = $2^{12} - 1 = 4095$ RS words
- 10% error-correcting code: 409 parity and 3686 data RS words



Error correction (after)

Evaluation

Environment	Bit rate	Error rate	Noise
Native	75.10 KBps	0.00%	–

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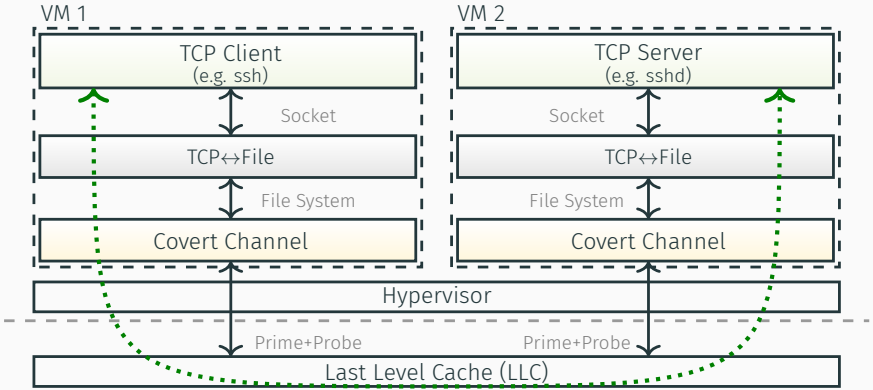
Evaluation

Environment	Bit rate	Error rate	Noise
Native	75.10 KBps	0.00%	–
Native	36.03 KBps	0.00%	`stress -m 1`
Amazon EC2	45.25 KBps	0.00%	–
Amazon EC2	45.09 KBps	0.00%	web server serving files on sender VM
Amazon EC2	42.96 KBps	0.00%	`stress -m 2` on sender VM
Amazon EC2	42.26 KBps	0.00%	`stress -m 1` on receiver VM
Amazon EC2	37.42 KBps	0.00%	web server on all 3 VMs, `stress -m 4` on 3rd VM, `stress -m 1` on sender and receiver VMs
Amazon EC2	34.27 KBps	0.00%	`stress -m 8` on third VM

Building an SSH connection



SSH evaluation

Between two instances on Amazon EC2

Noise	Connection
No noise	✓
`stress -m 8` on third VM	✓
Web server on third VM	✓
Web server on SSH server VM	✓
Web server on all VMs	✓
`stress -m 1` on server side	unstable

SSH evaluation

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No noise	✓
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`stress -m 1` on server side	unstable

Telnet also works with occasional corrupted bytes with `stress -m 1`

Cache covert channels: Take-away

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#2. Side-Channel Attack on Crypto

Side-channel attack on AES T-Tables implementation

- AES T-Tables: fast software implementation

D. A. Osvik et al. “Cache Attacks and Countermeasures: the Case of AES”. In: *CT-RSA 2006*. 2006.

Side-channel attack on AES T-Tables implementation

- AES T-Tables: fast software implementation
- uses precomputed look-up tables

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Side-channel attack on AES T-Tables implementation

- AES T-Tables: fast software implementation
- uses precomputed look-up tables
- one-round known-plaintext attack by Osvik et al.
  - p plaintext and k secret key
  - intermediate state $x^{(r)} = (x_0^{(r)}, \ldots, x_{15}^{(r)})$ at each round r
  - first round, accessed table indices are

$$x_i^{(0)} = p_i \oplus k_i \qquad \text{for all } i = 0, \ldots, 15$$

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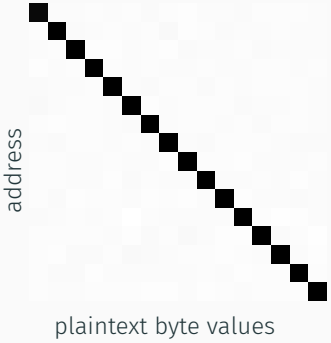
$$x_i^{(0)} = p_i \oplus k_i \qquad \text{for all } i = 0, \ldots, 15$$

$\rightarrow$ recovering accessed table indices $\Rightarrow$ recovering the key

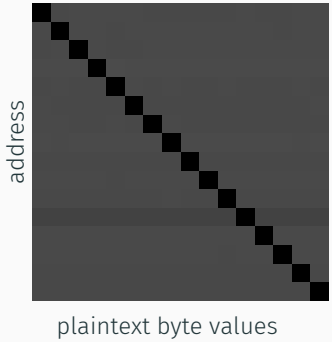
D. A. Osvik et al. "Cache Attacks and Countermeasures: the Case of AES". In: *CT-RSA 2006*. 2006.

Side-channel attack on AES T-Tables implementation

- monitoring which T-Table entry is accessed ($k_0 = \texttt{0x00}$)



Flush+Reload



Prime+Probe

Side-channel attack on AES T-Tables implementation

- it's an old attack...

M. Lipp et al. "ARMageddon: Cache Attacks on Mobile Devices". In: *USENIX Security Symposium*. 2016.

Side-channel attack on AES T-Tables implementation

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Side-channel attack on AES T-Tables implementation

- it's an old attack...
- everything should be fixed by now...
- Bouncy Castle on Android $\rightarrow$ default implementation uses T-Tables

M. Lipp et al. "ARMageddon: Cache Attacks on Mobile Devices". In: *USENIX Security Symposium*. 2016.

More attacks

- Flush+Reload
  - RSA: 96.7% of secret key bits in a single signature (Yarom et al.)
  - AES: full key recovery in 30000 dec. (a few seconds) (Guelmezoglu et al.)
- Prime+Probe
  - El Gamal (sliding window): full key recovery in 12 min. (Liu et al.)

Y. Yarom et al. “Flush+Reload: a High Resolution, Low Noise, L3 Cache Side-Channel Attack”. In: *USENIX Security Symposium*. 2014

B. Gülmezoglu et al. “A Faster and More Realistic Flush+Reload Attack on AES”. In: *COSADE'15*. 2015

F. Liu et al. “Last-Level Cache Side-Channel Attacks are Practical”. In: *S&P'15*. 2015.

Side-channel attack on crypto: Take-away

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- you should never write crypto with secret-dependent memory accesses
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- e.g., really hard to use AES T-Tables by mistake on OpenSSL
- big issue is adoption and legacy code still running

#3. Side-Channel Attack on Keystroke Timings

Cache Template Attacks

- locating event-dependent memory access $\rightarrow$ Cache Template Attacks

D. Gruss et al. “Cache Template Attacks: Automating Attacks on Inclusive Last-Level Caches”. In: *USENIX Security Symposium*. 2015.

Cache Template Attacks

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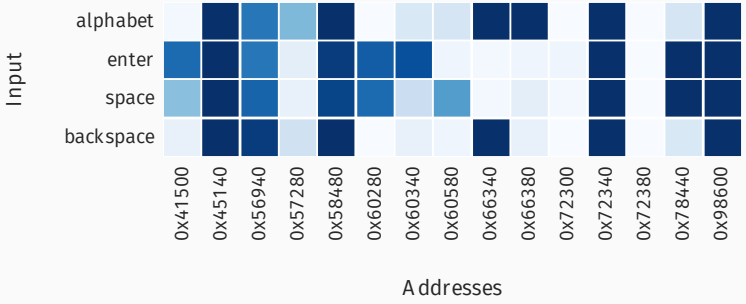
  3. repeat step 2 for every address

D. Gruss et al. "Cache Template Attacks: Automating Attacks on Inclusive Last-Level Caches". In: *USENIX Security Symposium*. 2015.

Which addresses to monitor?

- cache template matrix
  = how many cache hits for each pair (event, address)?



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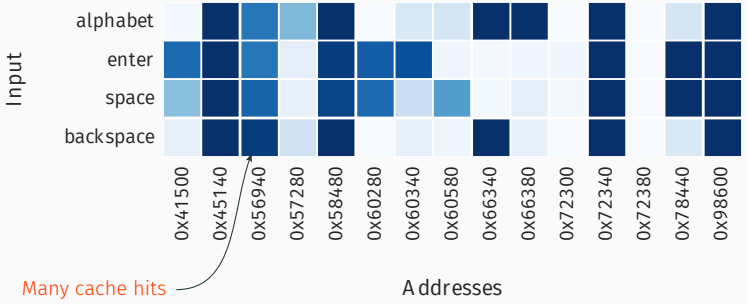

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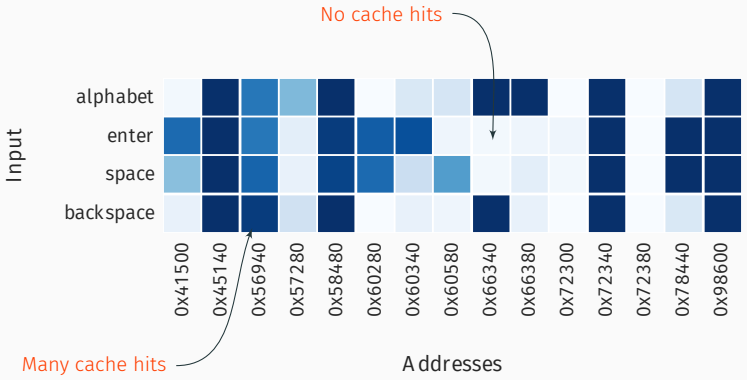
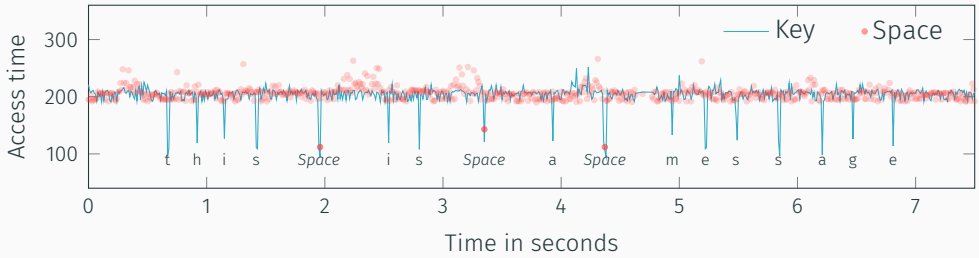


Spying on keystrokes

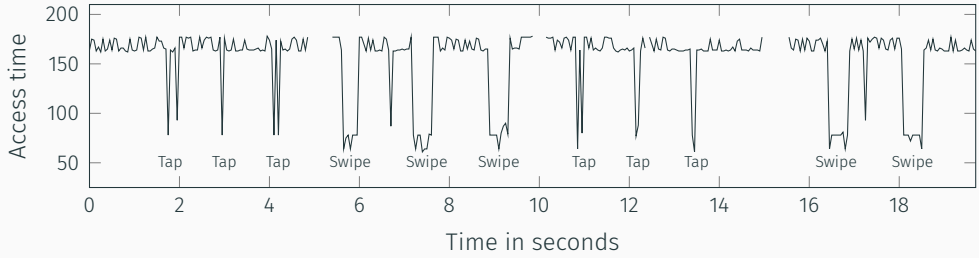
- Flush+Reload and Evict+Reload: fine-grained attacks → spy on keystrokes
- high-resolution timers → precise inter-keystroke timing
- next step: infer typed words with Hidden Markov Models



M. Lipp et al. "ARMageddon: Cache Attacks on Mobile Devices". In: *USENIX Security Symposium*. 2016

Differentiating events

- distinguishing between different types of events by monitoring access time



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- but the attack also allows distinguishing key groups

→ reduces search space for, e.g., password retrieval

#4. Side-Channel Attack on KASLR

`prefetch` instructions

`prefetch` fetches the line of data from memory containing the specified byte

6 `prefetch` instructions:

- `prefetcht0`: suggests CPU to load data into L1
- `prefetcht1`: suggests CPU to load data into L2
- `prefetcht2`: suggests CPU to load data into L3
- `prefetchnta`: suggests CPU to load data for non-temporal access
- `prefetchw`: suggests CPU to load data with intention to write
- `prefetchwt1`: suggests CPU to load vector data with intention to write

`prefetch` according to Intel

NOTE

Intel Corporation. *Intel® 64 and IA-32 Architectures Optimization Reference Manual*. 2014

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Using the PREFETCH instruction is recommended only if data does not fit in cache.

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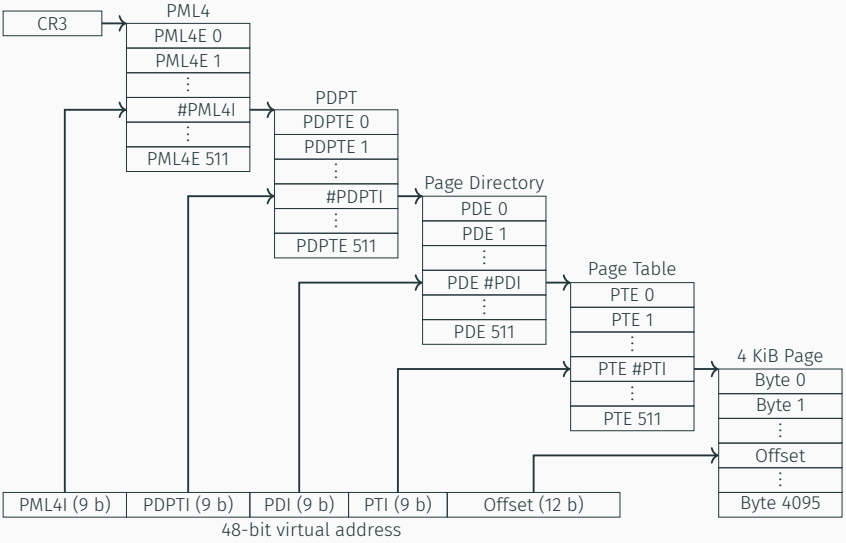
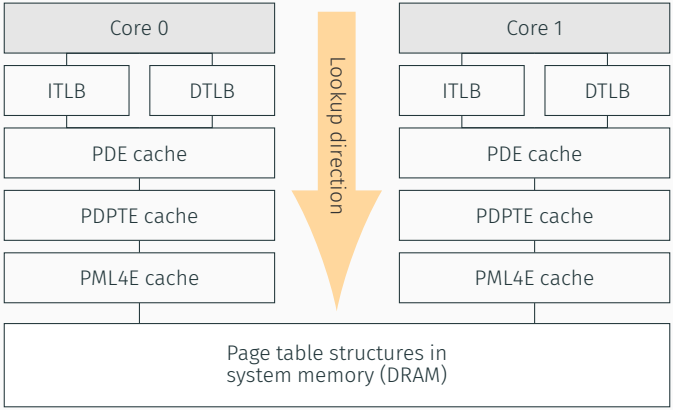
A little bit more background
before continuing...

Address translation

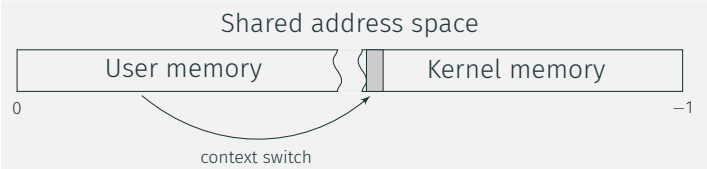


Address translation caches

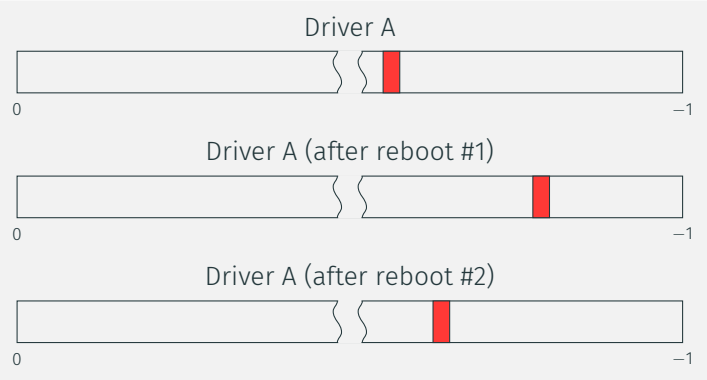


Kernel is mapped in every process

Today's operating systems:



Kernel Address Space Layout Randomization (KASLR)



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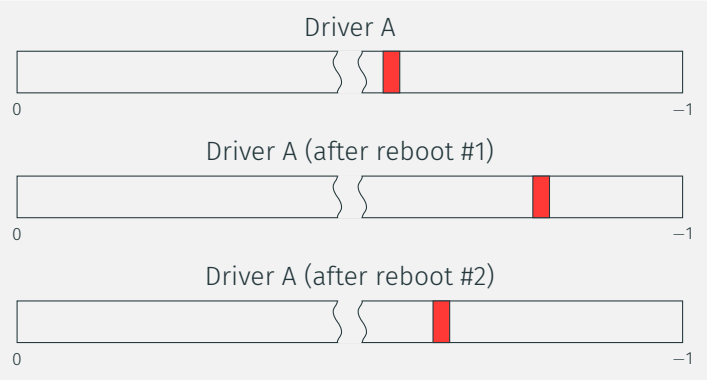
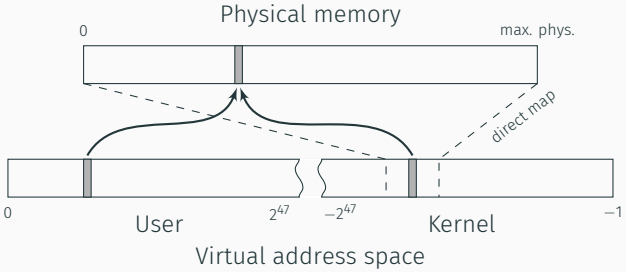


- same driver, different offset at each boot
- leaking kernel/driver addresses defeats KASLR

Kernel direct-physical map



- OS X, Linux, BSD, Xen PVM (Amazon EC2)

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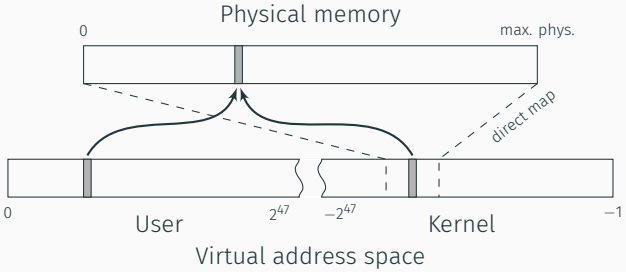

- OS X, Linux, BSD, Xen PVM (Amazon EC2)
- not Windows

Let's go back to `prefetch`!

`prefetch`: Unusual instructions (1)

- tells the CPU “I might need that later”

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Property #1: do not check privileges

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`prefetch`: Unusual instructions (2)

- operand is a virtual address

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Property #2: execution time varies

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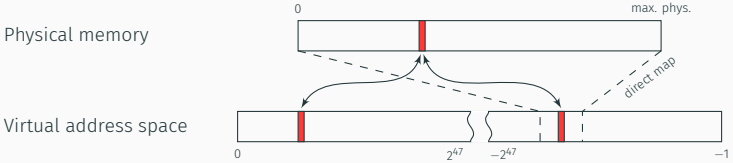
Address-translation oracle

Exploiting property #1 + kernel direct-physical map



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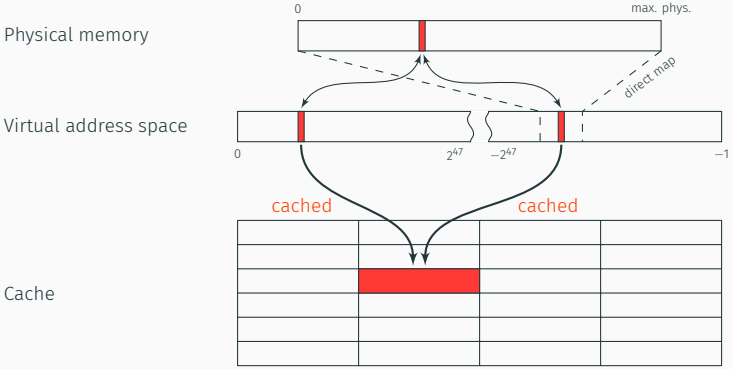

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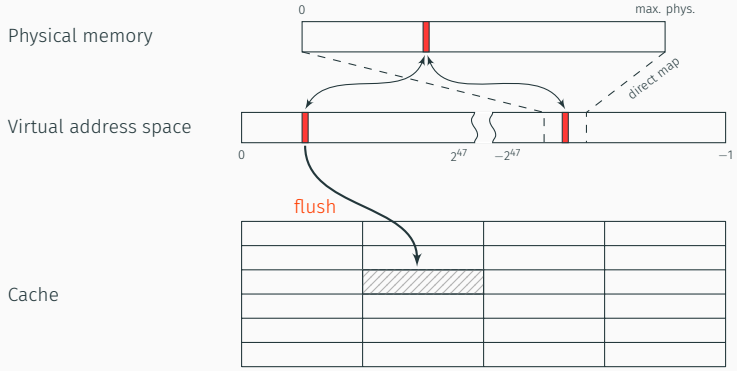

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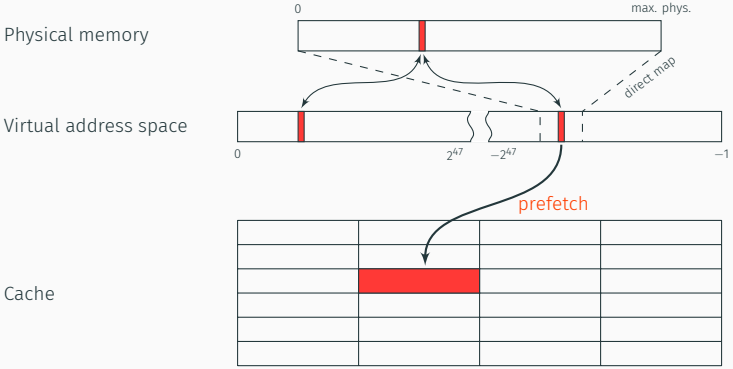

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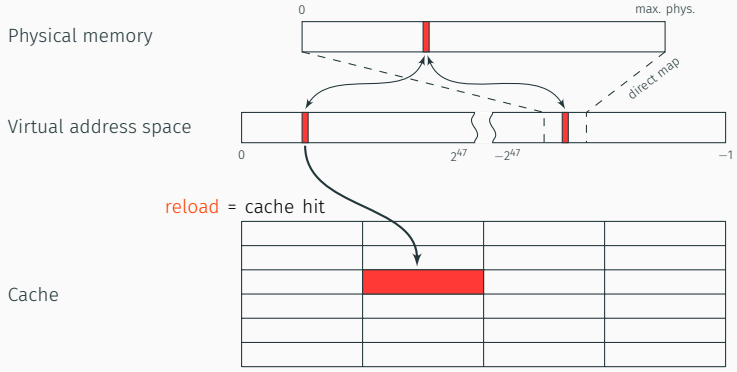
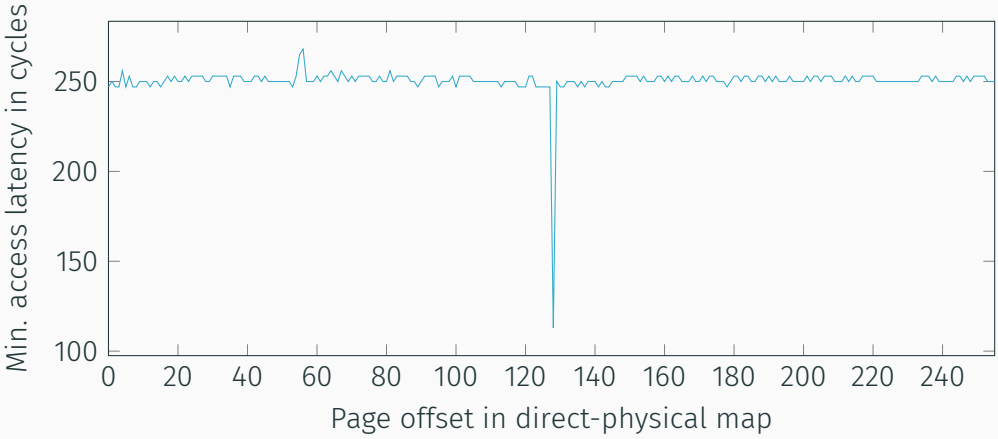


- cache hit → physical address in kernel mapping is the correct translation

Address-translation oracle



Translation-level oracle

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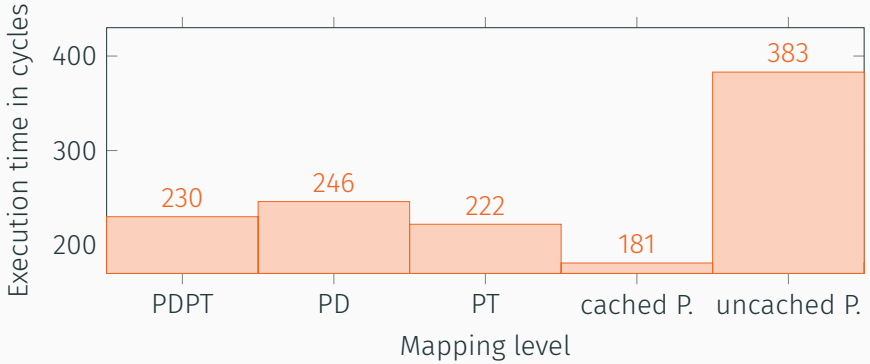

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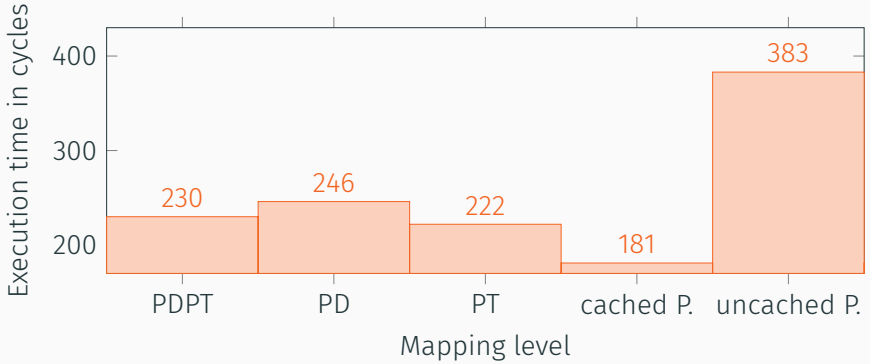

- timing depends on where the translation stops

Prefetch side-channel attacks

Using the two oracles

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- variants of cache attacks (e.g., Flush+Prefetch)

Prefetch side-channel attacks

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- translating virtual addresses to physical addresses (→ `/proc/pid/pagemap`)
  → now privileged → re-enables ret2dir exploits
- locating kernel drivers
  → bypasses KASLR

Defeating KASLR by locating kernel driver (1)

For all mapped pages, found with the translation-level oracle

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$\rightarrow$ fastest average access time is a driver page

Full attack on Windows 10 in $<$ 12 seconds

Defeating KASLR by locating kernel driver (2)

Prefetch side-channel attacks: Take-away

- `prefetch` does not allow you to access memory

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Prefetch side-channel attacks: Take-away

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- other microarchitectural attacks targeted KASLR
- still not completely dead

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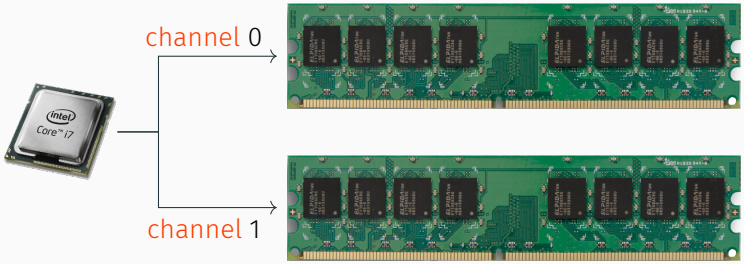
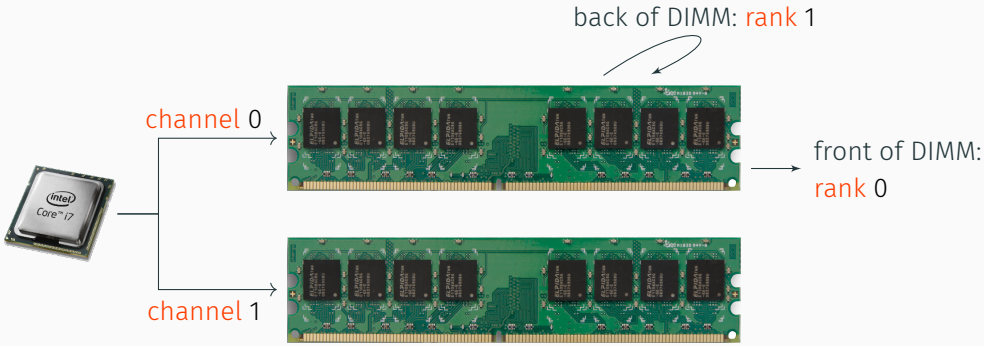
#5. Fault Attacks on DRAM in JavaScript

DRAM organization

DRAM organization



DRAM organization



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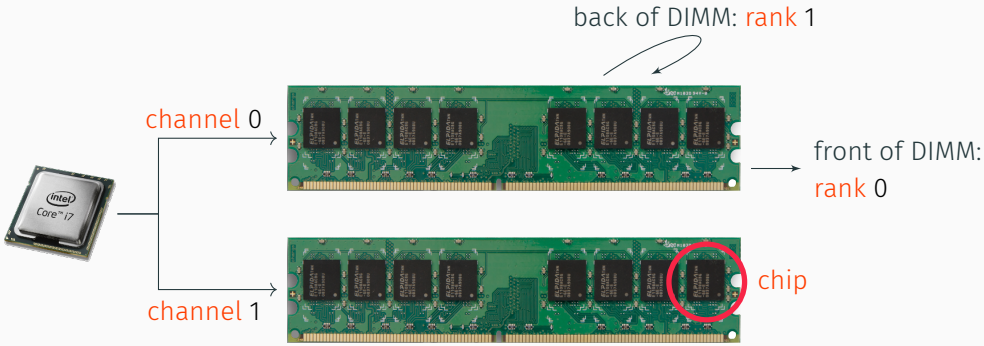
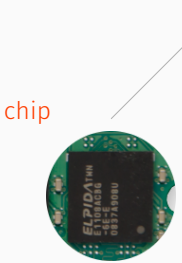
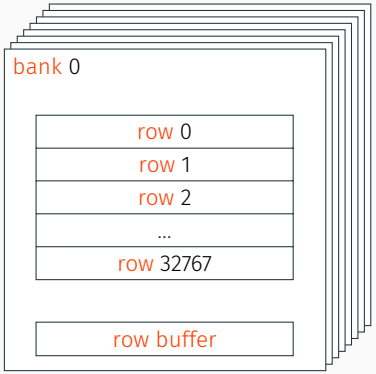


DRAM organization





- bits in cells in rows
- access: activate row, copy to row buffer

DRAM refresh

- cells leak $\rightarrow$ repetitive refresh necessary
- refresh $\approx$ reading (destructive) + writing same data again
- maximum interval between refreshes to guarantee data integrity

DRAM refresh

- cells leak → repetitive refresh necessary
- refresh ≈ reading (destructive) + writing same data again
- maximum interval between refreshes to guarantee data integrity

- cells leak faster upon proximate accesses → Rowhammer

Rowhammer

"It's like breaking into an apartment by repeatedly slamming a neighbor's door until the vibrations open the door you were after" – Motherboard Vice

Rowhammer

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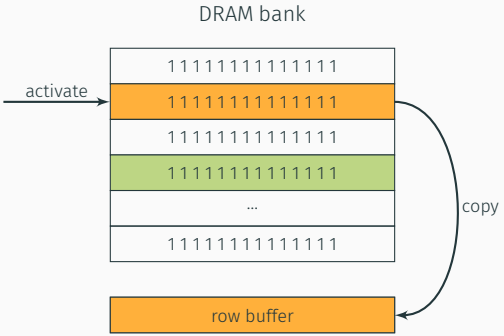

Rowhammer

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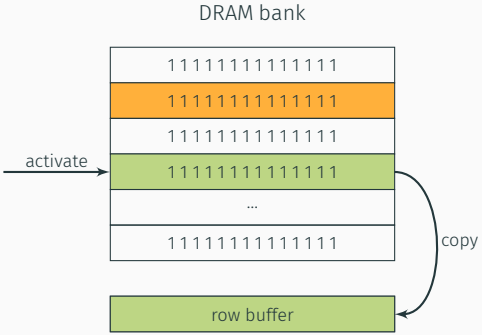

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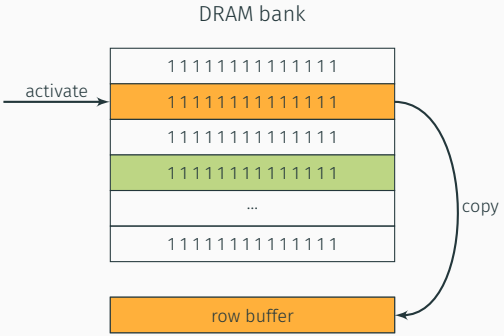

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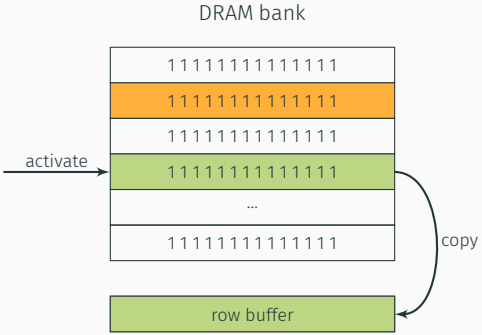

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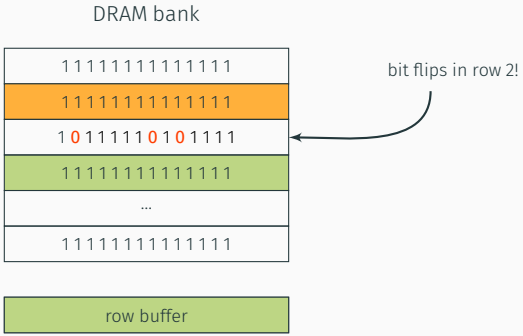
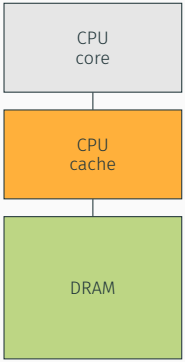


Impact of the CPU cache

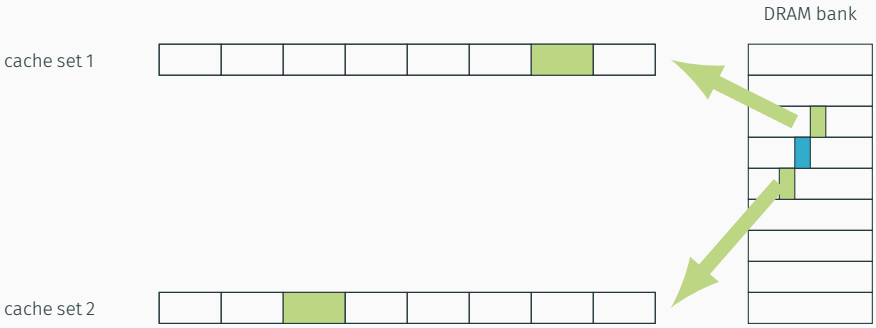


- only non-cached accesses reach DRAM
- original attacks use `clflush` instruction

→ flush line from cache

→ next access will be served from DRAM

Rowhammer (with `clflush`)



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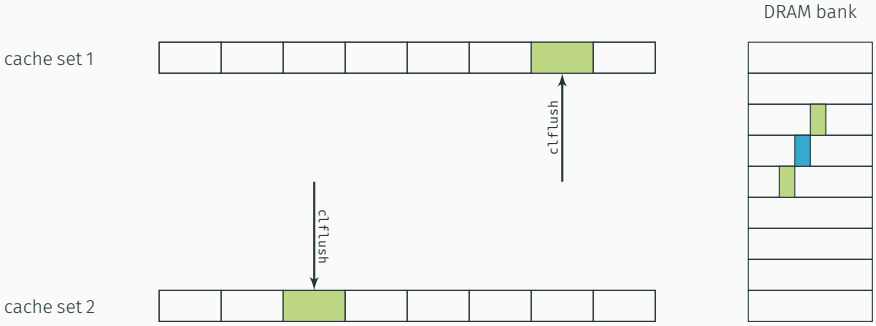

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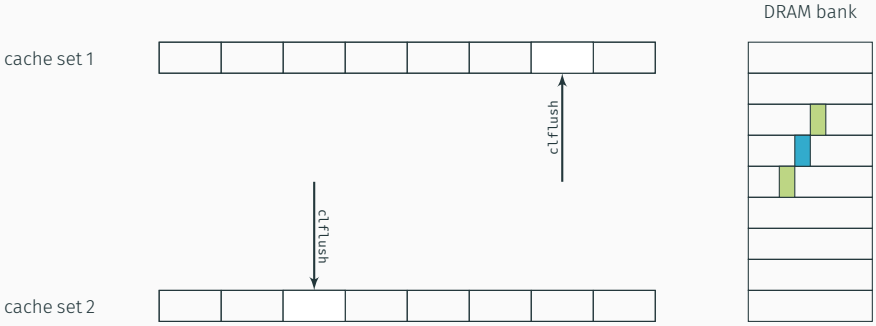

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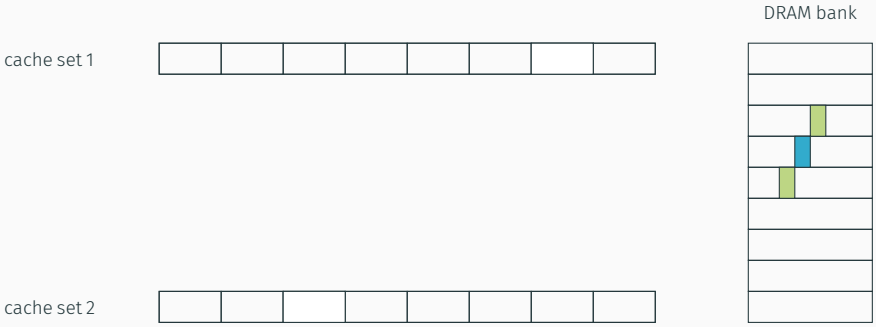

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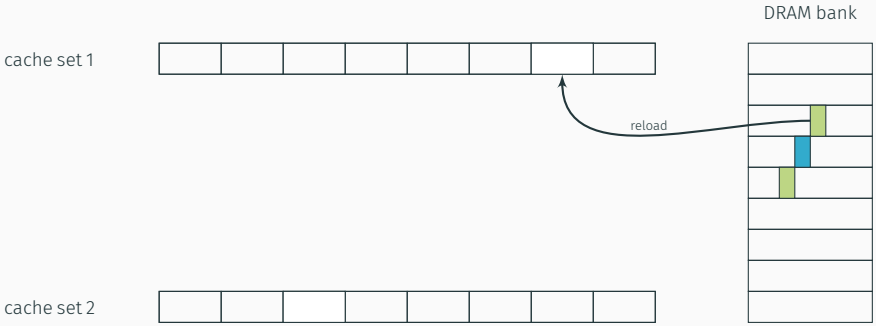

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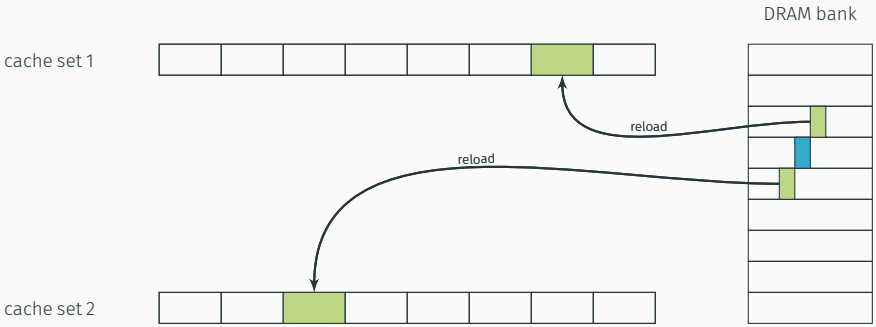

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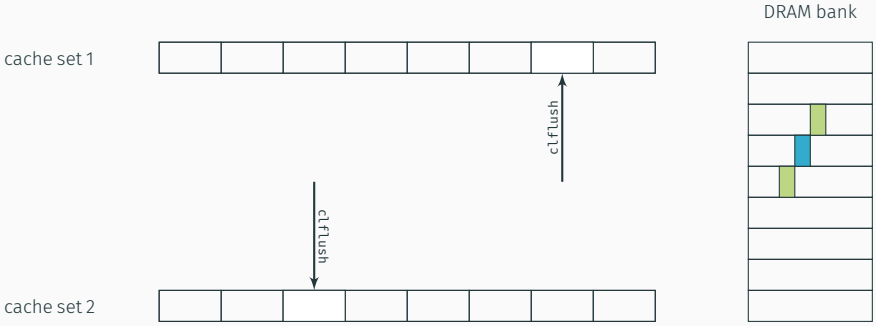

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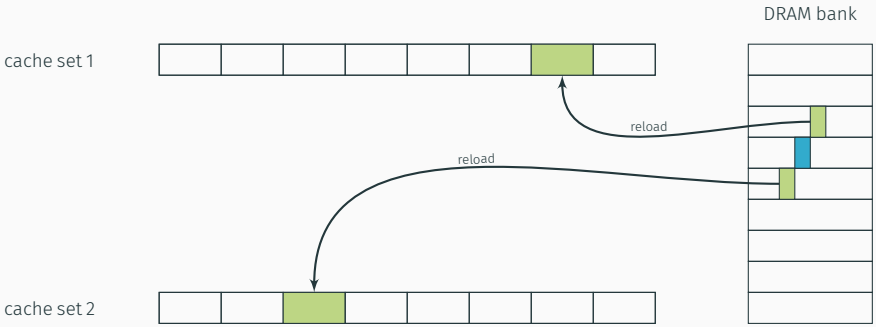

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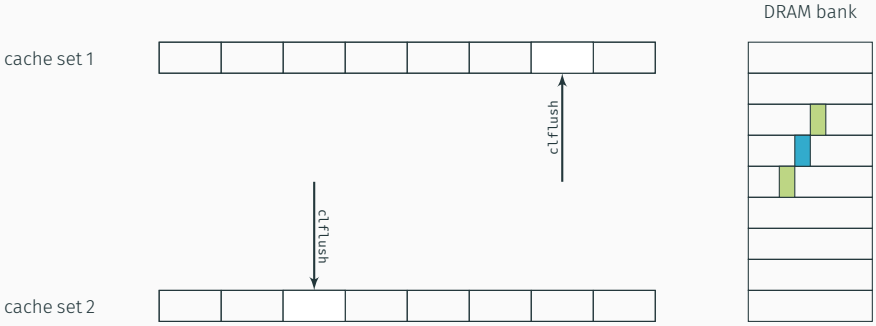

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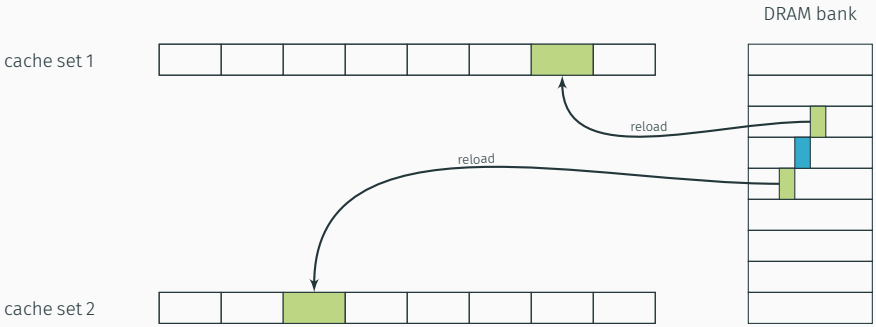

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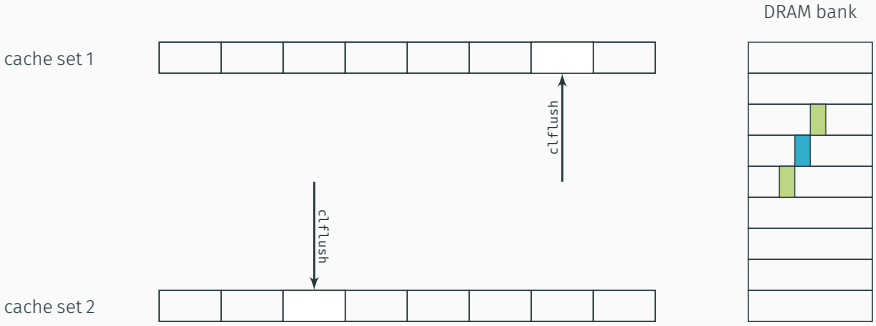

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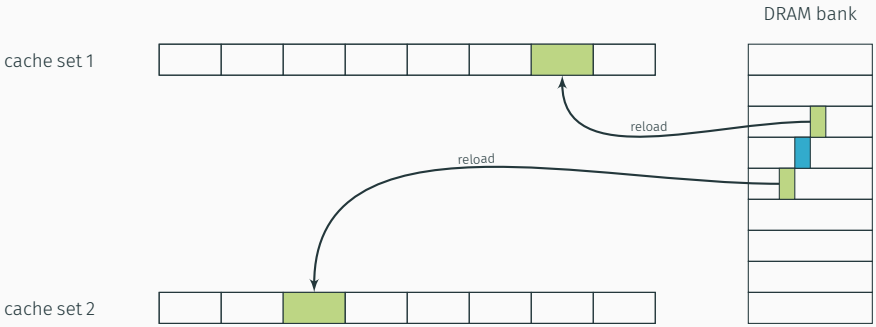

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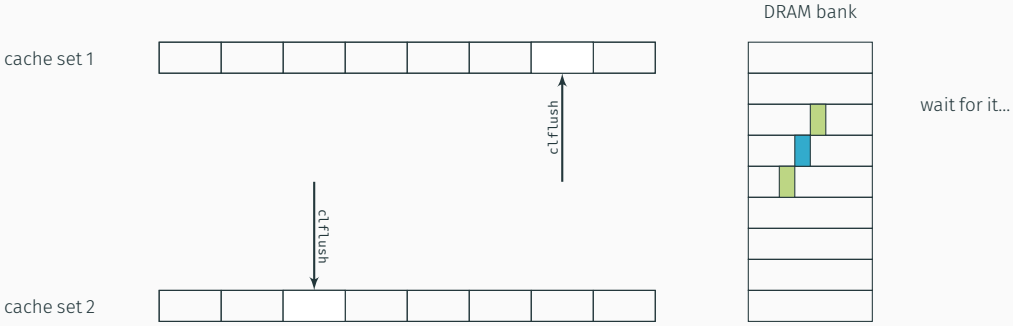

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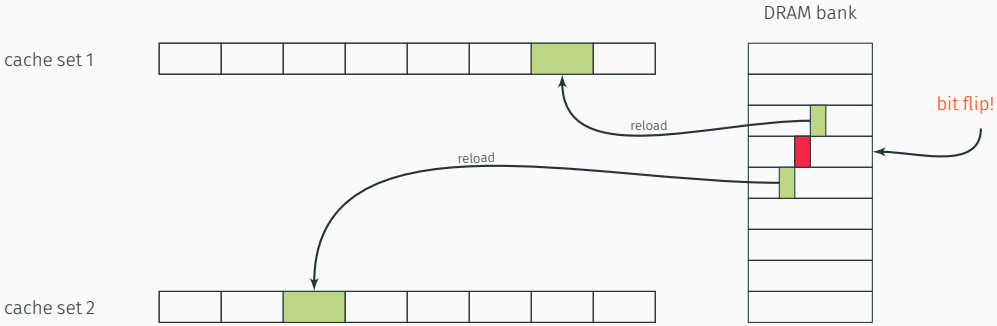

Flush, reload, flush, reload...

- the core of Rowhammer is essentially a Flush+Reload loop
- as much an attack on DRAM as on cache

Rowhammer without `clflush`?

- idea: avoid `clflush` to be independent of specific instructions
  $\rightarrow$ no `clflush` in JavaScript

D. Gruss et al. "Rowhammer.js: A Remote Software-Induced Fault Attack in JavaScript". In: *DIMVA'16*. 2016.

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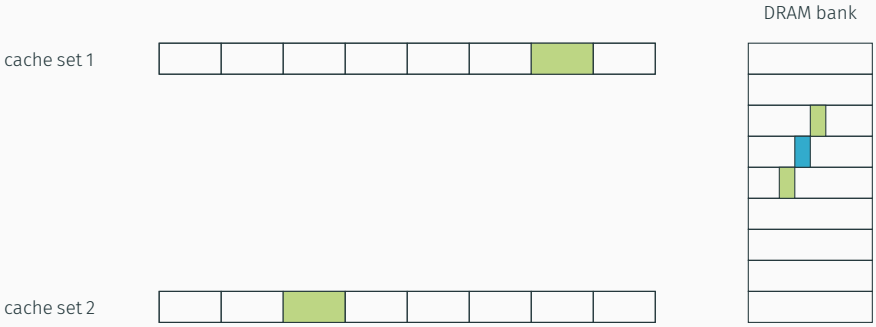

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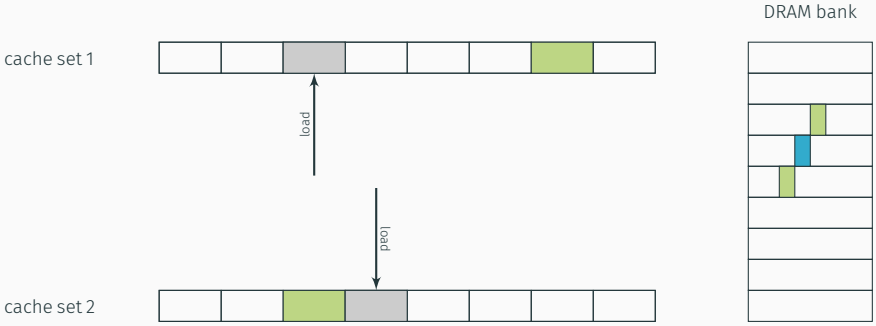

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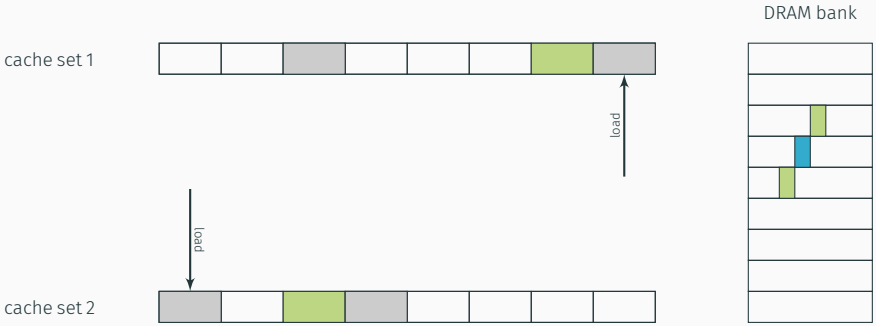

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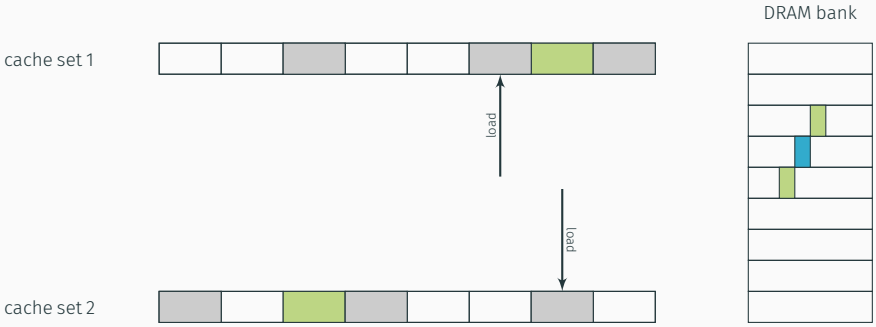

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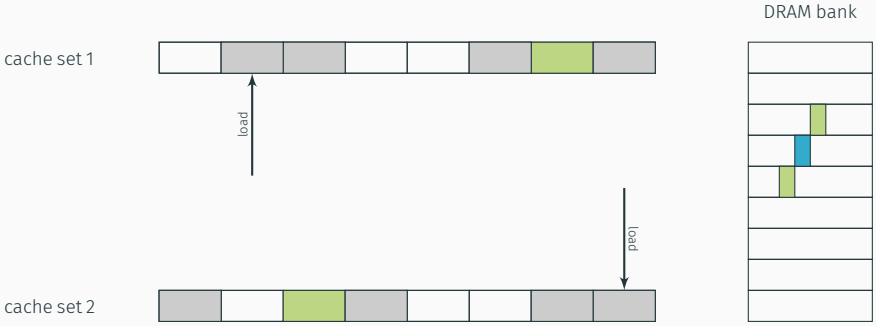

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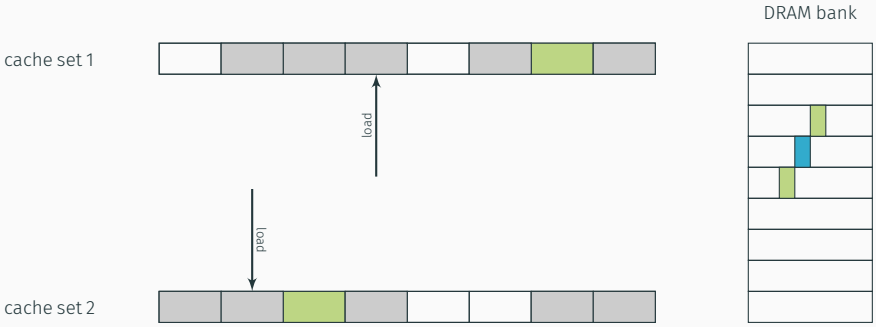

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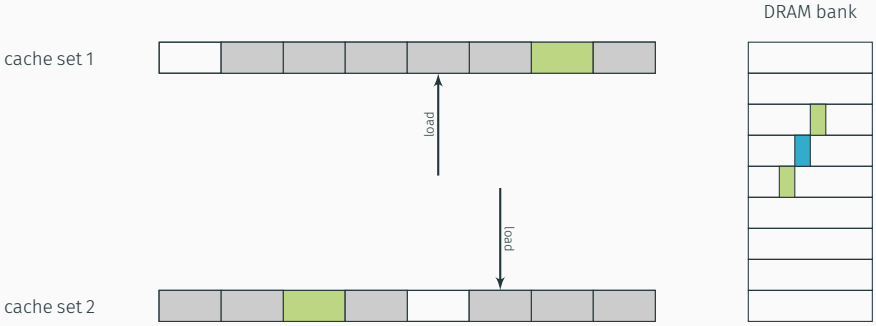

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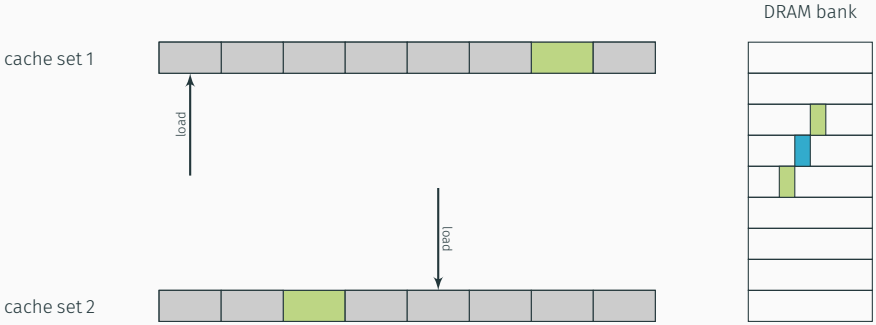

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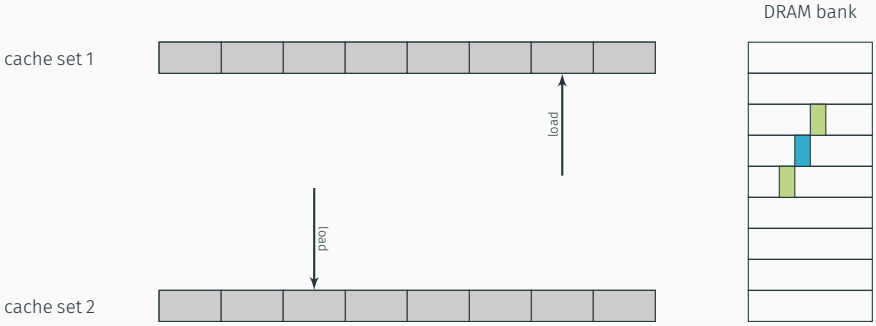

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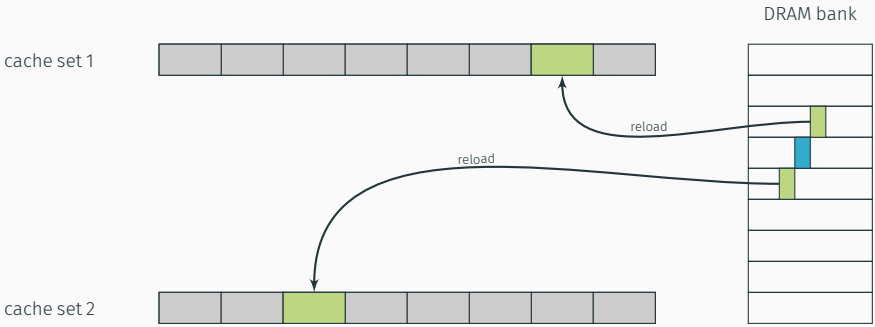

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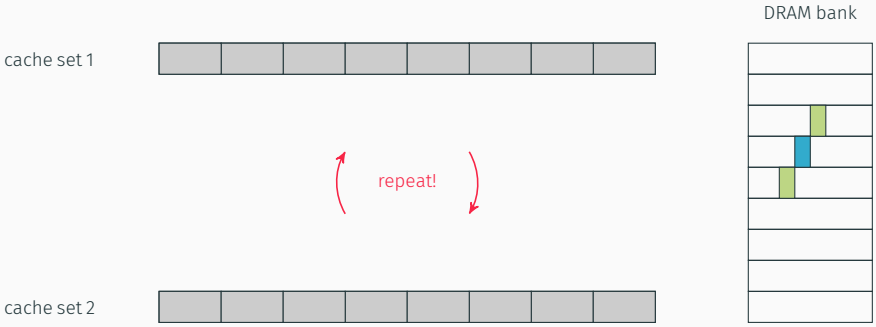

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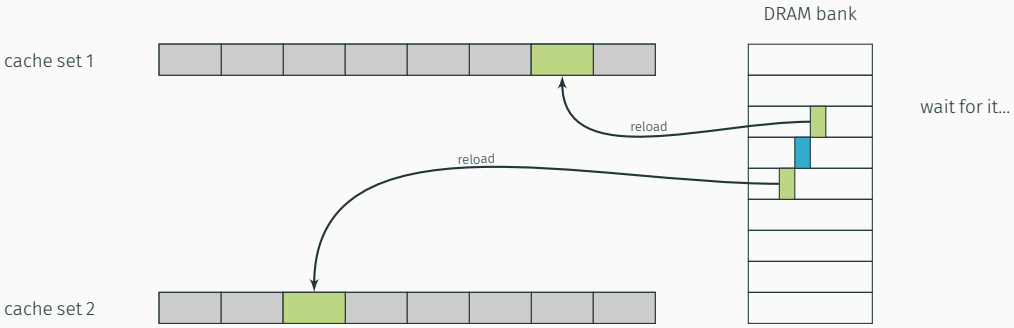

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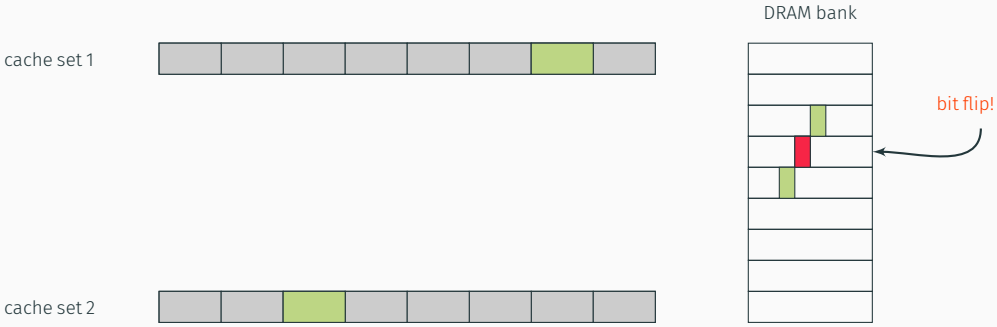
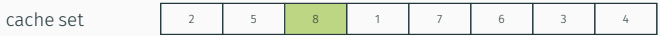


Replacement policy since Ivy Bridge

n accesses for an *n*-way cache



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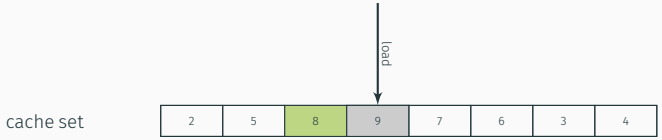

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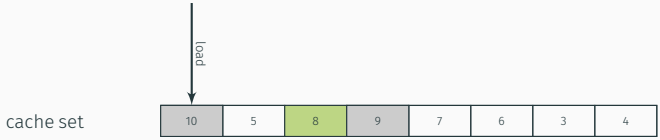

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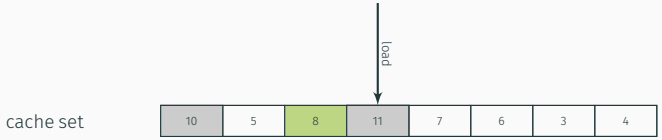

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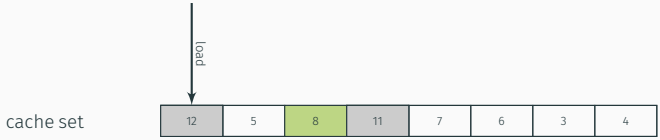

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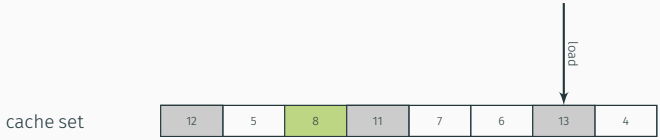

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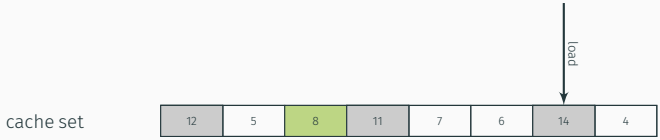

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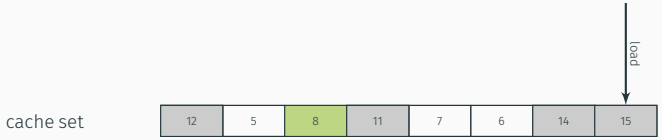

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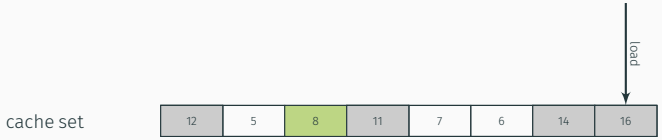

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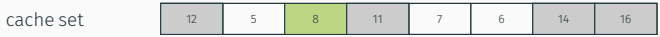

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- only 75% success rate on Haswell

Replacement policy since Ivy Bridge

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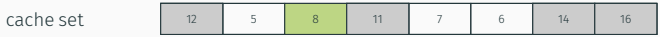

- no LRU replacement
- only 75% success rate on Haswell
- more accesses $\rightarrow$ higher success rate, but too slow

Requirements for Rowhammer

1. uncached memory accesses: need to reach DRAM
2. fast memory accesses: race against the next row refresh

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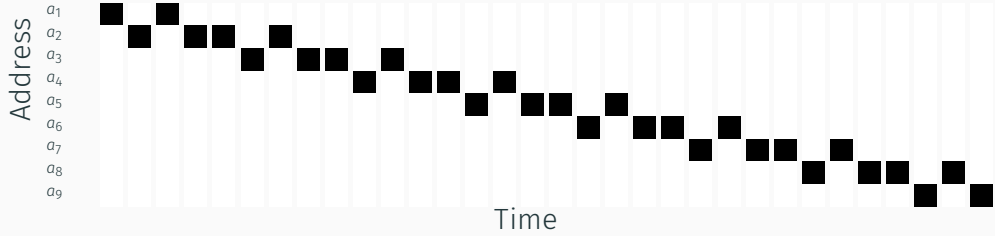
2. fast memory accesses: race against the next row refresh

$\rightarrow$ optimize the eviction rate and the timing

Cache eviction strategies: The beginning



$\rightarrow$ fast and effective on Haswell: eviction rate $>$99.97%

Cache eviction strategies: Evaluation

We evaluated more than 10000 strategies...

strategy	# accesses	eviction rate	loop time
$\mathscr{P}$-1-1-1-17	17		
$\mathscr{P}$-1-1-1-20	20		

Executed in a loop, on a Haswell with a 16-way last-level cache

Cache eviction strategies: Evaluation

We evaluated more than 10000 strategies...

strategy	# accesses	eviction rate	loop time
$\mathscr{P}$-1-1-1-17	17	74.46% ✗	
$\mathscr{P}$-1-1-1-20	20	99.82% ✓	

Executed in a loop, on a Haswell with a 16-way last-level cache

Cache eviction strategies: Evaluation

We evaluated more than 10000 strategies...

strategy	# accesses	eviction rate	loop time
$\mathscr{P}$-1-1-1-17	17	74.46% ✗	307 ns ✓
$\mathscr{P}$-1-1-1-20	20	99.82% ✓	934 ns ✗

Executed in a loop, on a Haswell with a 16-way last-level cache

Cache eviction strategies: Evaluation

We evaluated more than 10000 strategies...

strategy	# accesses	eviction rate	loop time
$\mathscr{P}$-1-1-1-17	17	74.46% ✗	307 ns ✓
$\mathscr{P}$-1-1-1-20	20	99.82% ✓	934 ns ✗
$\mathscr{P}$-2-1-1-17	34		

Executed in a loop, on a Haswell with a 16-way last-level cache

Cache eviction strategies: Evaluation

We evaluated more than 10000 strategies...

strategy	# accesses	eviction rate	loop time
$\mathscr{P}$-1-1-1-17	17	74.46% ✗	307 ns ✓
$\mathscr{P}$-1-1-1-20	20	99.82% ✓	934 ns ✗
$\mathscr{P}$-2-1-1-17	34	99.86% ✓	

Executed in a loop, on a Haswell with a 16-way last-level cache

Cache eviction strategies: Evaluation

We evaluated more than 10000 strategies...

strategy	# accesses	eviction rate	loop time
$\mathscr{P}$-1-1-1-17	17	74.46% ✗	307 ns ✓
$\mathscr{P}$-1-1-1-20	20	99.82% ✓	934 ns ✗
$\mathscr{P}$-2-1-1-17	34	99.86% ✓	191 ns ✓

Executed in a loop, on a Haswell with a 16-way last-level cache

Cache eviction strategies: Evaluation

We evaluated more than 10000 strategies...

strategy	# accesses	eviction rate	loop time
$\mathscr{P}$-1-1-1-17	17	74.46% ✗	307 ns ✓
$\mathscr{P}$-1-1-1-20	20	99.82% ✓	934 ns ✗
$\mathscr{P}$-2-1-1-17	34	99.86% ✓	191 ns ✓
$\mathscr{P}$-2-2-1-17	64		

Executed in a loop, on a Haswell with a 16-way last-level cache

Cache eviction strategies: Evaluation

We evaluated more than 10000 strategies...

strategy	# accesses	eviction rate	loop time
$\mathscr{P}$-1-1-1-17	17	74.46% ✗	307 ns ✓
$\mathscr{P}$-1-1-1-20	20	99.82% ✓	934 ns ✗
$\mathscr{P}$-2-1-1-17	34	99.86% ✓	191 ns ✓
$\mathscr{P}$-2-2-1-17	64	99.98% ✓	

Executed in a loop, on a Haswell with a 16-way last-level cache

Cache eviction strategies: Evaluation

We evaluated more than 10000 strategies...

strategy	# accesses	eviction rate	loop time
$\mathscr{P}$-1-1-1-17	17	74.46% ✗	307 ns ✓
$\mathscr{P}$-1-1-1-20	20	99.82% ✓	934 ns ✗
$\mathscr{P}$-2-1-1-17	34	99.86% ✓	191 ns ✓
$\mathscr{P}$-2-2-1-17	64	99.98% ✓	180 ns ✓

Executed in a loop, on a Haswell with a 16-way last-level cache

Cache eviction strategies: Evaluation

We evaluated more than 10000 strategies...

strategy	# accesses	eviction rate	loop time
$\mathscr{P}$-1-1-1-17	17	74.46% ✗	307 ns ✓
$\mathscr{P}$-1-1-1-20	20	99.82% ✓	934 ns ✗
$\mathscr{P}$-2-1-1-17	34	99.86% ✓	191 ns ✓
$\mathscr{P}$-2-2-1-17	64	99.98% ✓	180 ns ✓

→ more accesses, smaller execution time?

Executed in a loop, on a Haswell with a 16-way last-level cache

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Time in ns

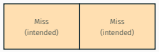
Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)



$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Time in ns

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Time in ns

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

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Time in ns

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Time in ns

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Time in ns

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Time in ns

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$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

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Time in ns

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

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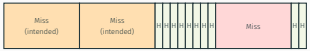

Time in ns

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Time in ns

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

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Cache eviction strategies: Illustration

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Time in ns

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Time in ns

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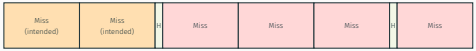
Time in ns

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

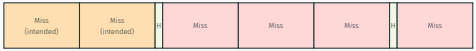


$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Time in ns

Cache eviction strategies: Illustration

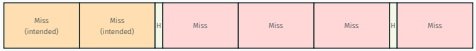
$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)



$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Cache eviction strategies: Illustration

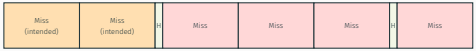
$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)



$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)



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Cache eviction strategies: Illustration

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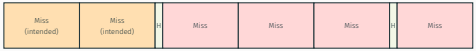
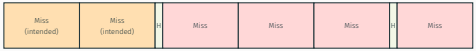


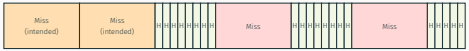
$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)



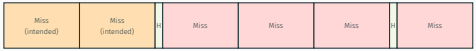
$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)



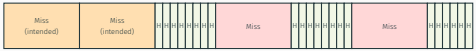
Time in ns

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)



$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)



Time in ns

Cache eviction strategies: Illustration

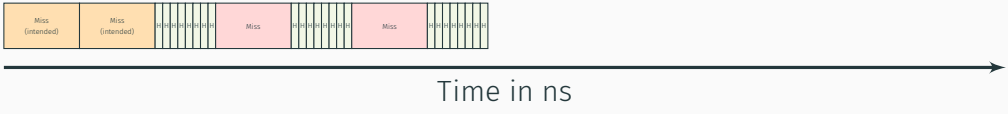
$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Cache eviction strategies: Illustration

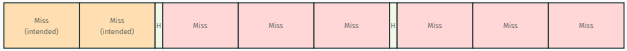
$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)



Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)



$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Cache eviction strategies: Illustration

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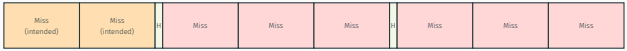

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Cache eviction strategies: Illustration

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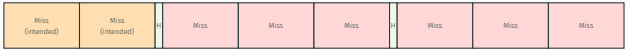

$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Cache eviction strategies: Illustration

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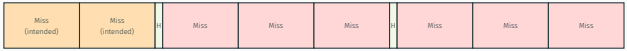

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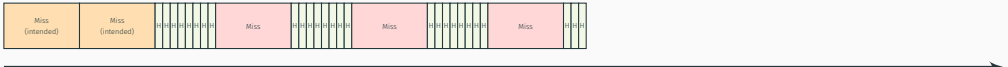

Cache eviction strategies: Illustration

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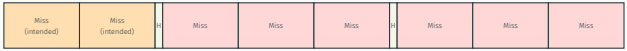

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Cache eviction strategies: Illustration

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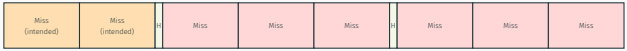
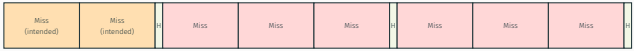


$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)



$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

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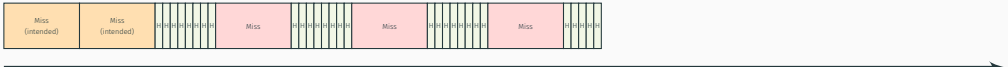

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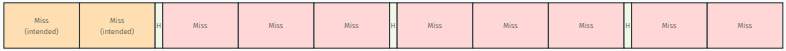

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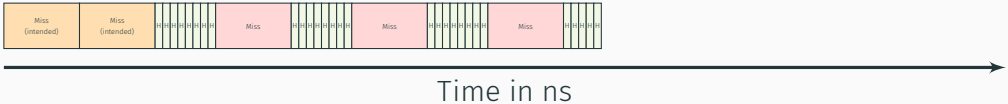


Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Time in ns

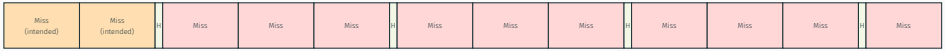
Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)



$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Time in ns

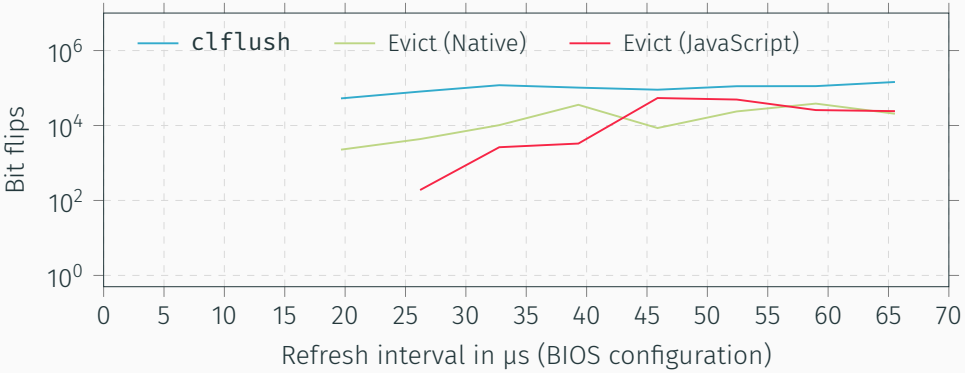
Cache eviction strategies: Illustration

$\mathscr{P}$-1-1-1-17 (17 accesses, 307ns)

$\mathscr{P}$-2-1-1-17 (34 accesses, 191ns)

Time in ns

Evaluation on Haswell



Number of bit flips within 15 minutes.

Rowhammer.js: Take-Away

- cache eviction fast enough to replace `clflush`
- independent of programming language and available instructions

E. Bosman et al. “Dedup Est Machina: Memory Deduplication as an Advanced Exploitation Vector”. In: *S&P’16*. 2016

Rowhammer.js: Take-Away

- cache eviction fast enough to replace `clflush`
- independent of programming language and available instructions
- lessons learned from side channels to perform a fault attack

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Rowhammer.js: Take-Away

- cache eviction fast enough to replace `clflush`
- independent of programming language and available instructions
- lessons learned from side channels to perform a fault attack
- first remote fault attack, from a browser

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Rowhammer.js: Take-Away

- cache eviction fast enough to replace `clflush`
- independent of programming language and available instructions
- lessons learned from side channels to perform a fault attack
- first remote fault attack, from a browser
- if you think a fault is not exploitable, think again

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Countermeasures

Countermeasures

- different levels: hardware, system, application
- different goals
  - remove interferences
  - add noise to interferences
  - make it impossible to measure interferences

Hardware level: Fixing the instruction set?

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  - unprivileged line eviction

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→ attacks still possible (e.g., Prime+Probe)

Hardware level: Stop sharing hardware?

- stop sharing cache

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- what about JavaScript attacks?

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Hardware level: Changes in microarchitecture

- secure cache designs: Random-Permutation Cache, Partition-Locked Cache

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→ performance and cost win, no implementation by manufacturers

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System level: Prevention

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  - → removing timers is not realistic

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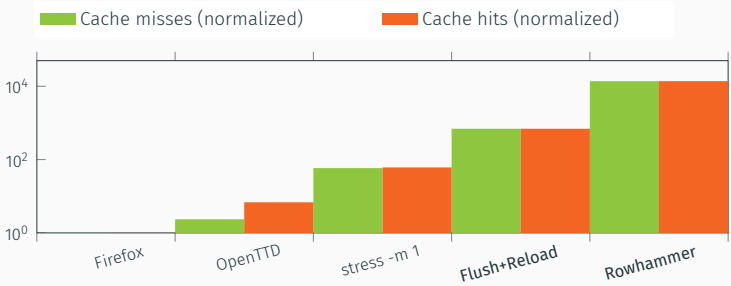
System level: Detect on-going attacks

- using performance counters to monitor cache hits and cache misses

→ risk of false positives



N. Herath et al. “These are Not Your Grand Daddys CPU Performance Counters – CPU Hardware Performance Counters for Security”. In: *Black Hat 2015 Briefings*. 2015

D. Gruss et al. “Flush+Flush: A Fast and Stealthy Cache Attack”. In: *DIMVA'16*. 2016

Application level: Detect leakage

- CacheAudit : static analysis of source code
- Cache Template Attacks : dynamic approach

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→ see Boris' talk this afternoon!

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- square-and-multiply-always algorithm
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- hardware implementations (AES-NI, etc.)

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- hardware implementations (AES-NI, etc.)

→ protecting crypto is possible and necessary!

→ a few CVEs that have been treated: CVE-2005-0109, CVE-2013-4242, CVE-2014-0076, CVE-2016-0702, CVE-2016-2178

Bigger Perspective and Conclusions

`rdseed` and floating point operations

- `rdseed`
  - request a random seed to the hardware random number generator
  - fixed number of precomputed random bits, takes time to regenerate them

  $\rightarrow$ covert channel

D. Evtyushkin et al. “Covert Channels through Random Number Generator: Mechanisms, Capacity Estimation and Mitigations”. In: *CCS’16*. 2016

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  → covert channel
- `fadd`, `fmul`
  - floating-point unit
  - floating point operations running time depends on the operands

  → bypassing Firefox's same origin policy via SVG filter timing attack

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`jmp` and TSX instructions

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  - branch prediction and branch target prediction → branch prediction unit

  → covert channels, side-channel attacks on crypto, bypassing kernel ASLR

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- TSX instructions
  - extension for transactional memory support in hardware

  → bypassing kernel ASLR

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→ looking forward to Boris' talk this afternoon!

Questions?

Contact

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@BloodyTangerine

Cache attacks:
Software side-channel and fault attacks

Clémentine Maurice, Graz University of Technology

May 11, 2017—Spring school on Security & Correctness in the IoT 2017