Microarchitectural Attacks in the Cloud

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Cloud abstracts physical resources to the user

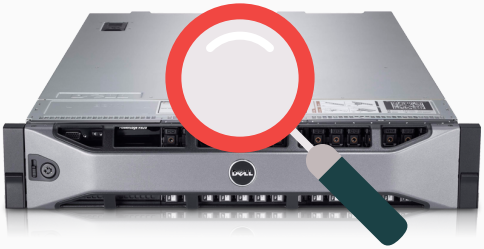
Logical isolation maintained by the hypervisor

Cloud abstracts physical resources to the user

Logical isolation maintained by the hypervisor

But there is a real physical world behind this abstraction

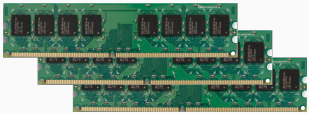
server



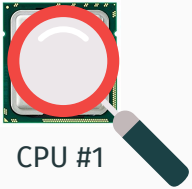
server

CPU #1

CPU #2



DRAM



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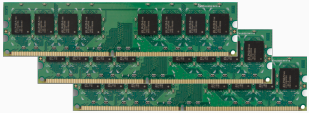

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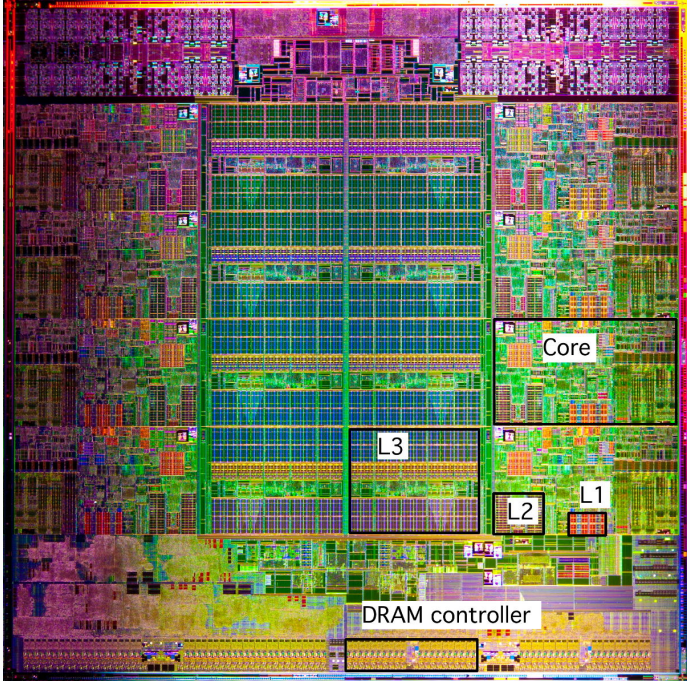
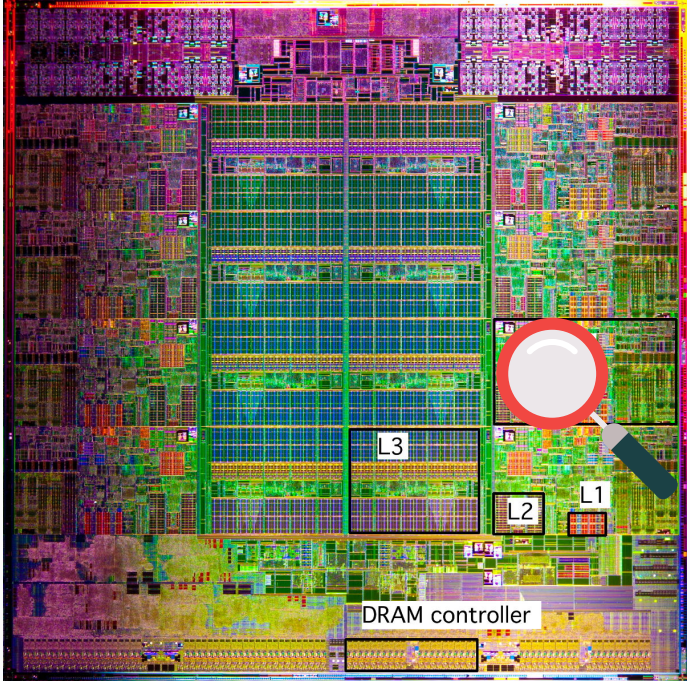

Core
L3
L2
L1
DRAM controller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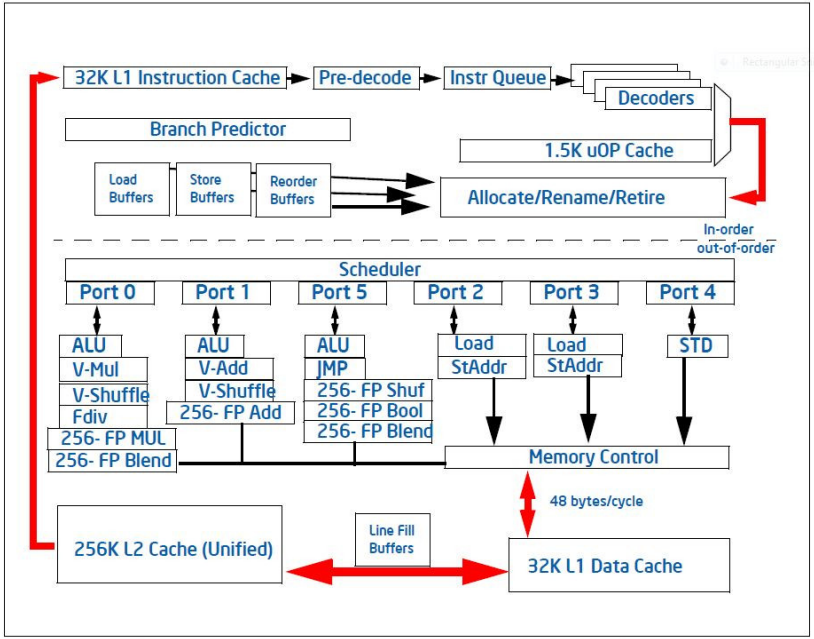
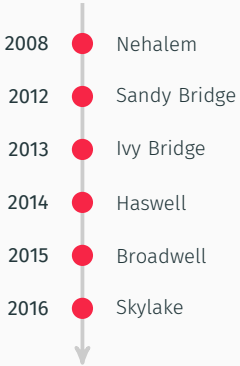


Figure 2-1. Intel microarchitecture code name Sandy Bridge Pipeline Functionality

Microarchitectural Side-Channel Attacks

From small optimizations...



- new microarchitectures yearly

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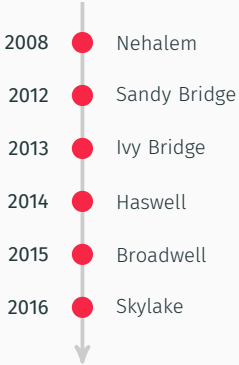

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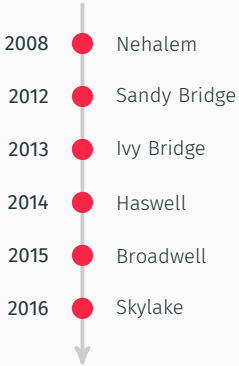

- new microarchitectures yearly
- performance improvement $\approx 5\%$
- very small optimizations: caches, branch prediction...

... To microarchitectural side-channel attacks

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- microarchitectural side channels come from these optimizations
- several processes are sharing microarchitectural components
- attacker infers information from a victim process via hardware usage
- pure-software attacks by unprivileged processes
- sequences of benign-looking actions $\rightarrow$ hard to detect

Same-Core Side-Channel Attacks

Hyper-threading

- threads sharing one core share resources: L1, L2 cache, branch predictor

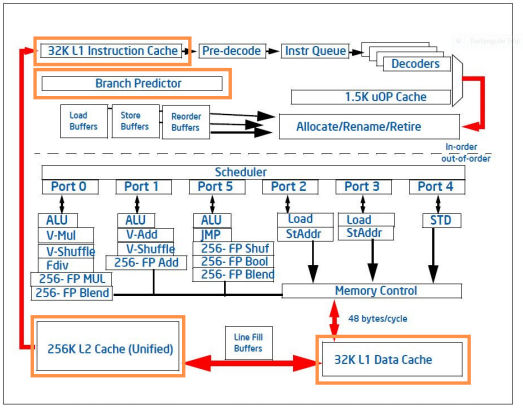

Figure 2-1. Intel microarchitecture code name Sandy Bridge Pipeline Functionality

Branch prediction (1/2)

- conditional branches → taking the branch or not depends on some condition
- the condition has to be evaluated
- instead of stalling the pipeline → speculative execution of one possible path

→ branch prediction unit predicts the most likely execution path

Branch prediction (2/2)

- branch prediction unit
  - branch target buffer (BTB): cache that stores the target addresses of previously executed branches
  - branch predictor: makes the prediction on the outcome of the branch

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- two things can go wrong
  1. BTB miss
  2. misprediction of the branch
- can be observed by timing penalty or hardware performance counters

Side channels on the branch prediction unit

- attacker and victim processes executed on the same core
- algorithm with secret-dependent path
- detect whether specific branches are taken or not taken

$S \leftarrow A \times B$
$S \leftarrow (S - (S \times N - 1 \mod R) \times N)/R$
if $S > N$ **then**
    $S \leftarrow S - N$
return S

Side channel on the BTB

- attacker forces the eviction of victim's entries in the BTB
- next victim execution → BTB miss → forces a prediction *not-taken*
- if the branch is in fact *taken* → misprediction → update the BTB
- next attacker execution → entries not in the BTB anymore

→ attacker's BTB misses used to deduce victim's branch mispredictions

O. Acıiçmez, J.-P. Seifert, and c. K. Koç. "Predicting secret keys via branch prediction". In: *CT-RSA 2007*. 2007

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- requires to know how the BTB is indexed (undocumented)
- in most cases micro-benchmarks can extract enough information

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Easy solution #1

Possible side channels using components shared by a core?

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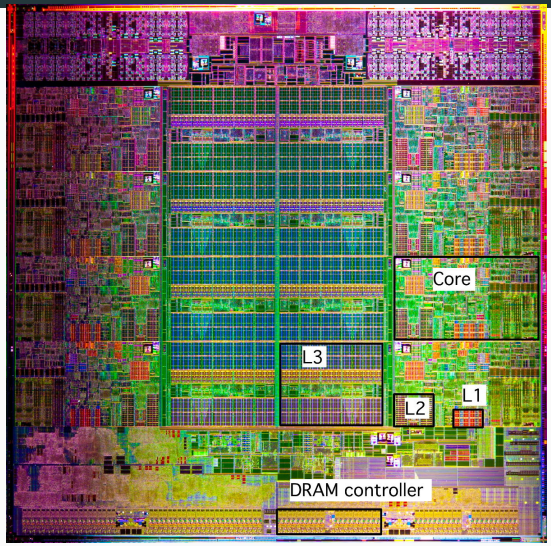
Possible side channels using components shared by a core?

Stop sharing a core!

Cross-Core Side-Channel Attacks

Caches on Intel CPUs



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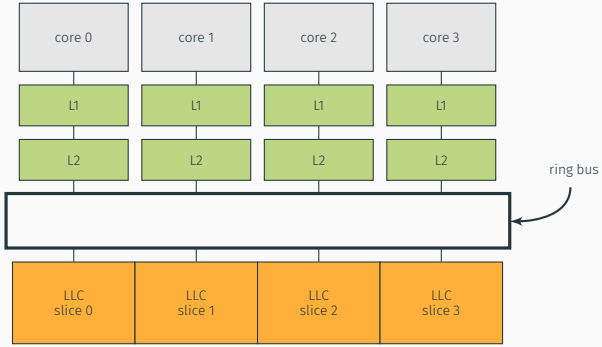

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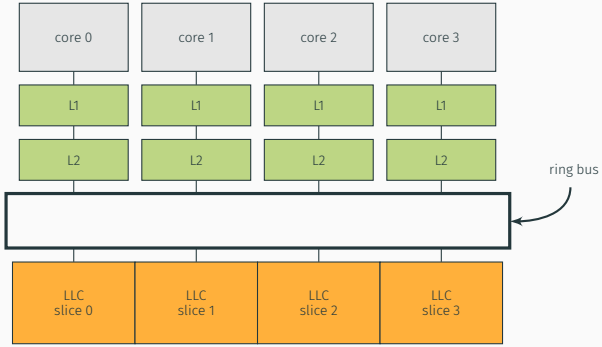

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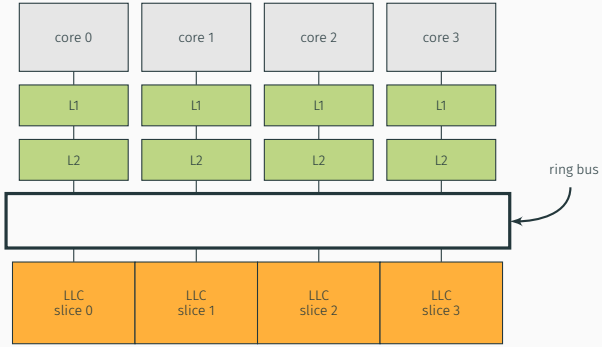

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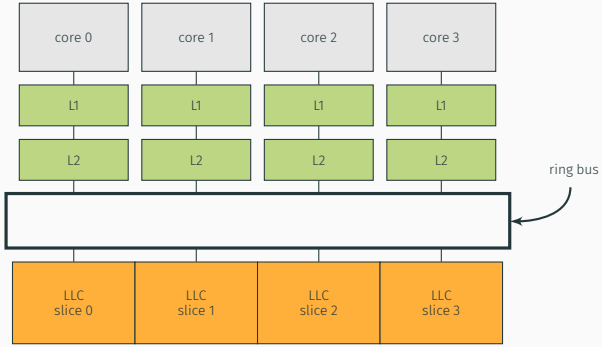

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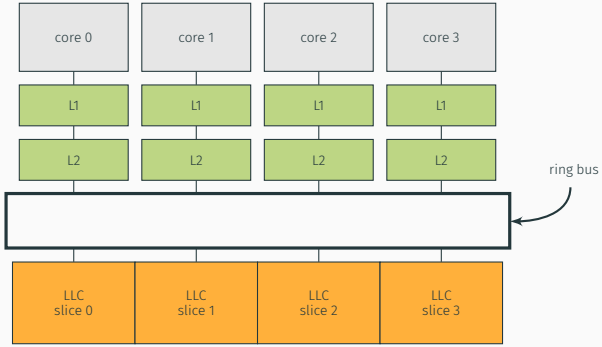

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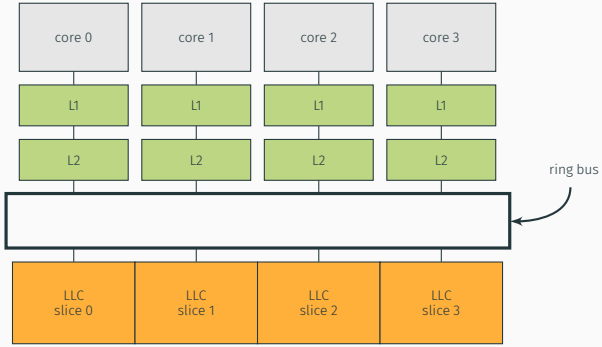

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- last-level cache
  - divided in slices
  - shared across cores
  - inclusive

Set-associative caches

Cache

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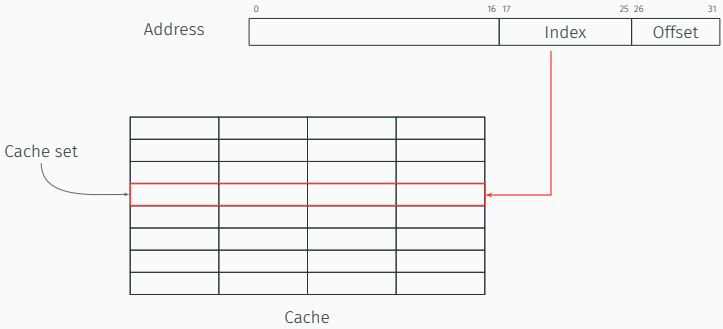
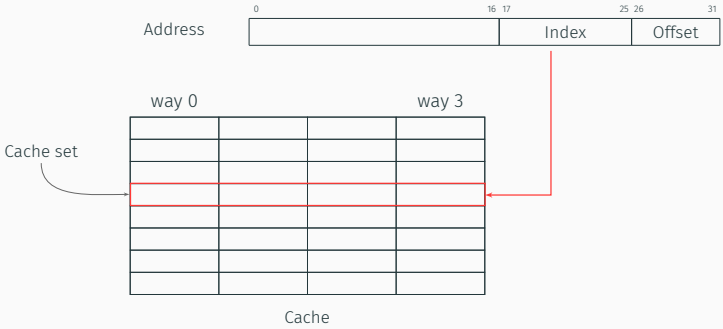


Data loaded in a specific set depending on its address

Set-associative caches



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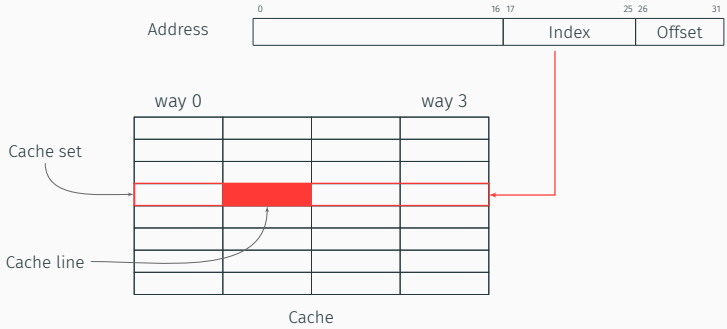

Data loaded in a specific set depending on its address

Several ways per set

Cache line loaded in a specific way depending on the replacement policy

Cache attacks

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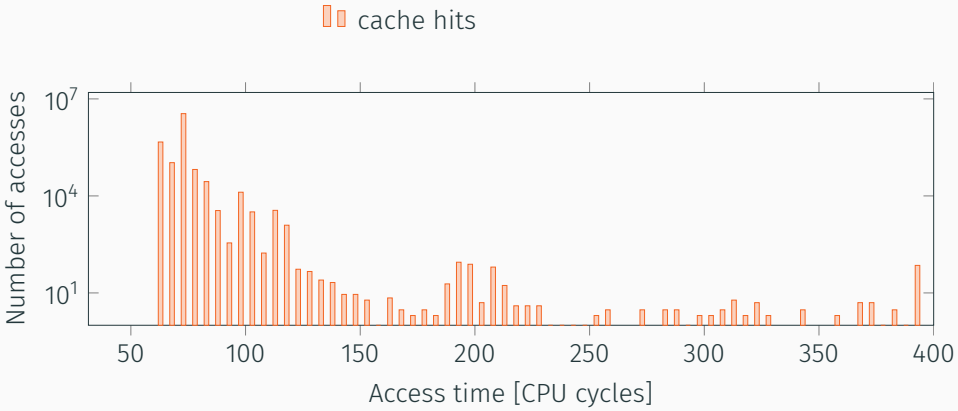
- cache attacks leverage this timing difference

Timing differences



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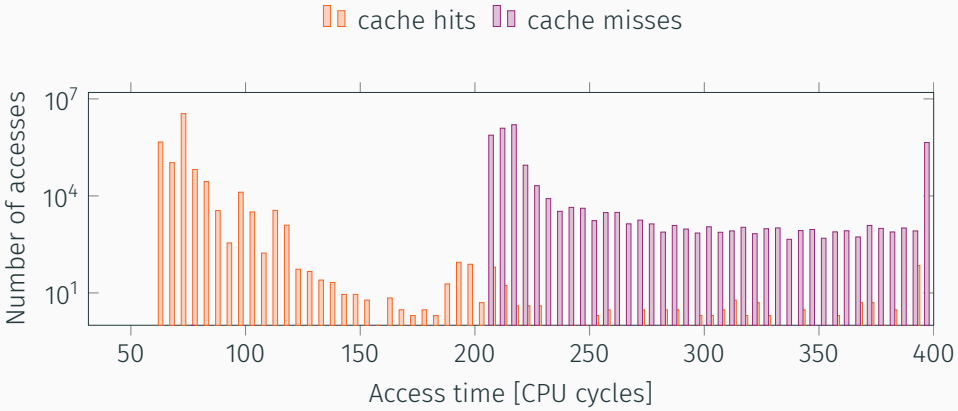
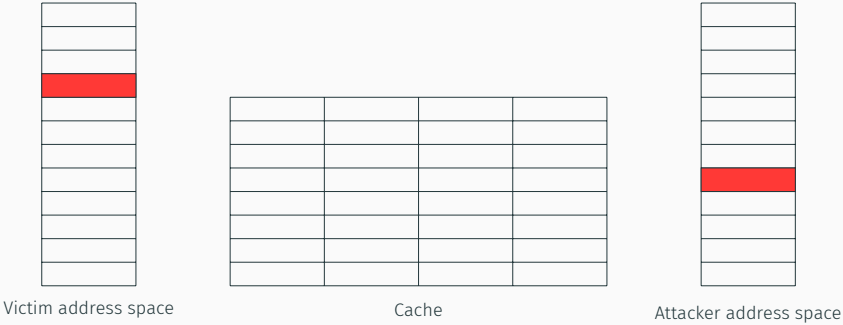


Cache attacks: Flush+Reload



Step 1: Attacker maps shared library (shared memory, in cache)

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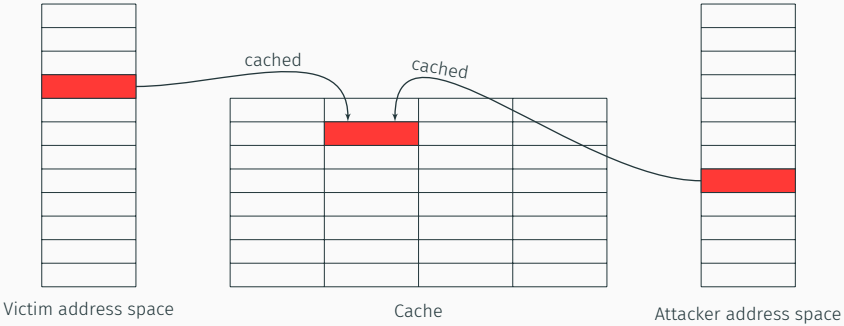

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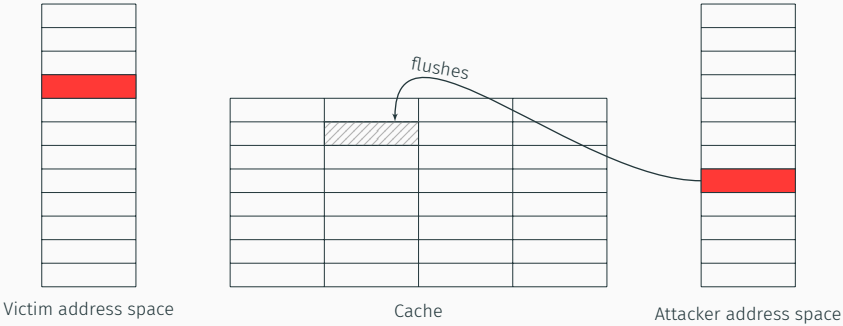

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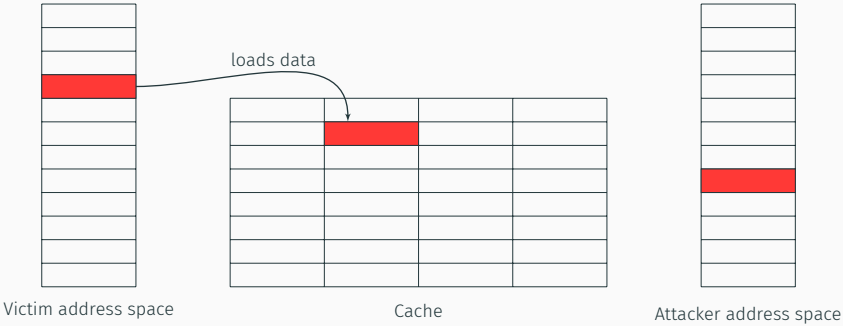

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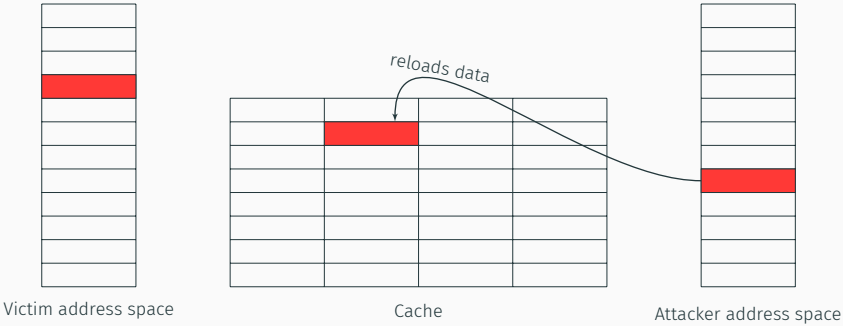

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Step 4: Attacker reloads the data

Flush+Reload: Applications

- cross-VM side channel attacks on crypto algorithms
  - RSA: 96.7% of secret key bits in a single signature
  - AES: full key recovery in 30000 dec. (a few seconds)

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`https://github.com/IAIK/cache_template_attacks`

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  - RSA: 96.7% of secret key bits in a single signature
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- Cache Template Attacks: automatically finds information leakage

  $\rightarrow$ side channel on keystrokes and AES T-tables implementation

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→ memory deduplication between VMs

Easy solution #2

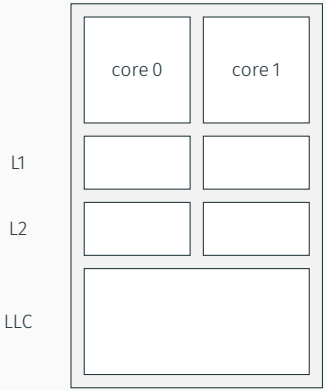
Possible side channels using memory deduplication?

Easy solution #2

Possible side channels using memory deduplication?

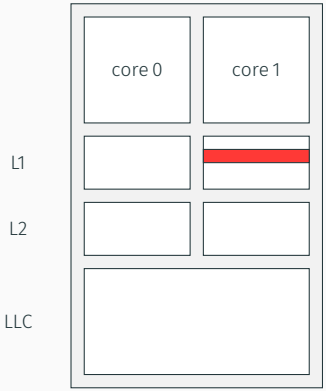
Disable memory deduplication!

Inclusive property



- inclusive LLC: superset of L1 and L2

Inclusive property



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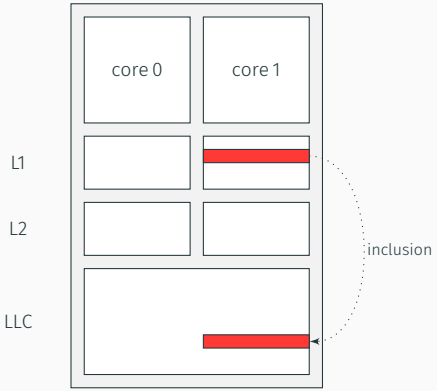

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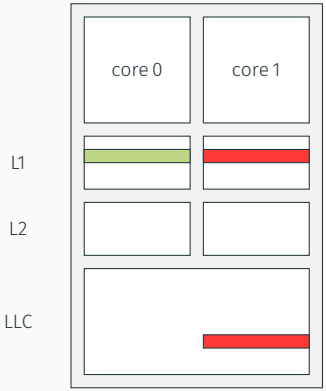

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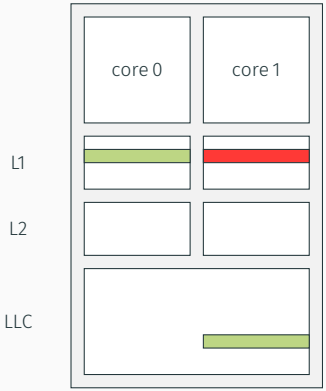

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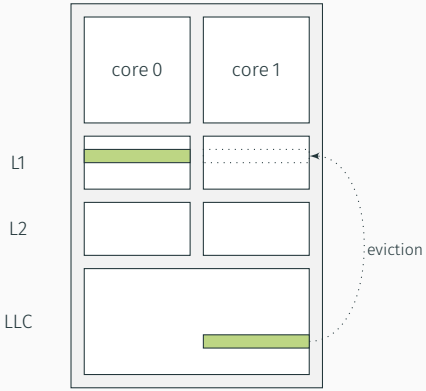

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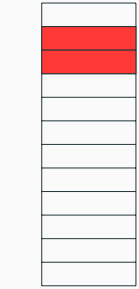
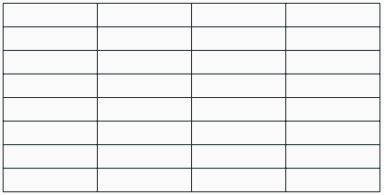
- data evicted from the LLC is also evicted from L1 and L2
- a core can evict lines in the private L1 of another core

Cache attacks: Prime+Probe



Victim address space



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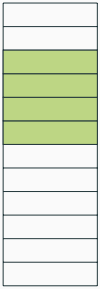

Attacker address space

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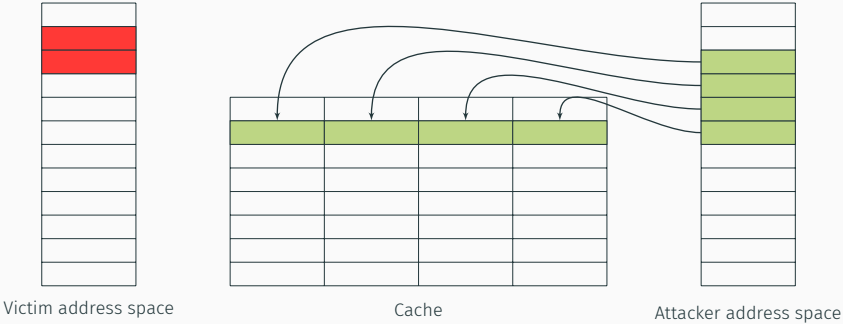

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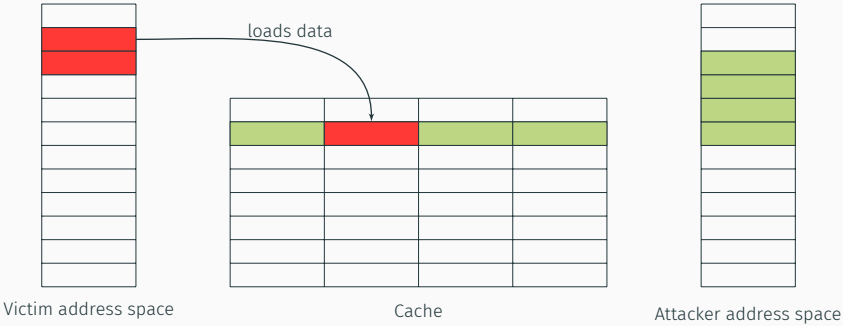

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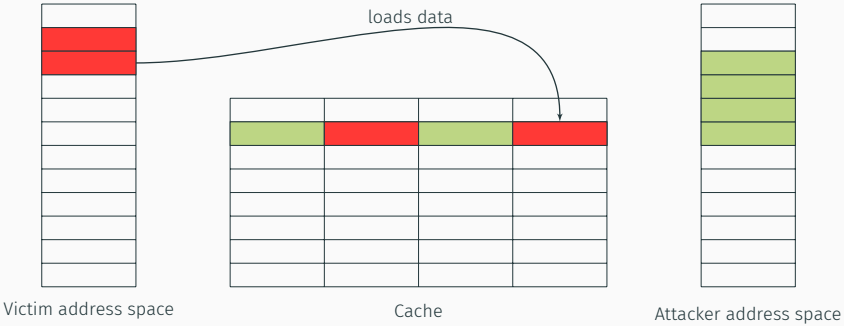
Step 2: Victim evicts cache lines while running

Cache attacks: Prime+Probe



Step 1: Attacker primes, *i.e.*, fills, the cache (no shared memory)

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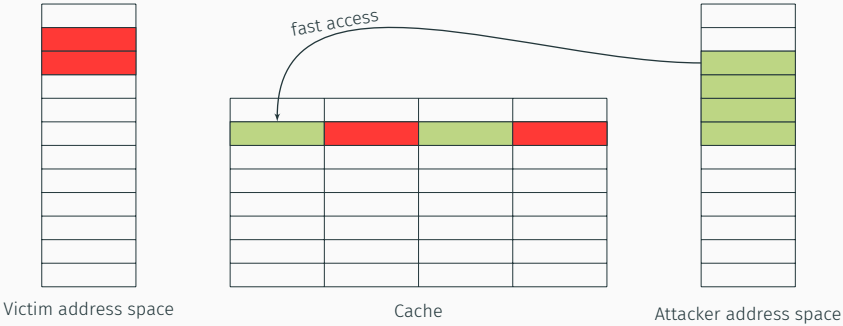

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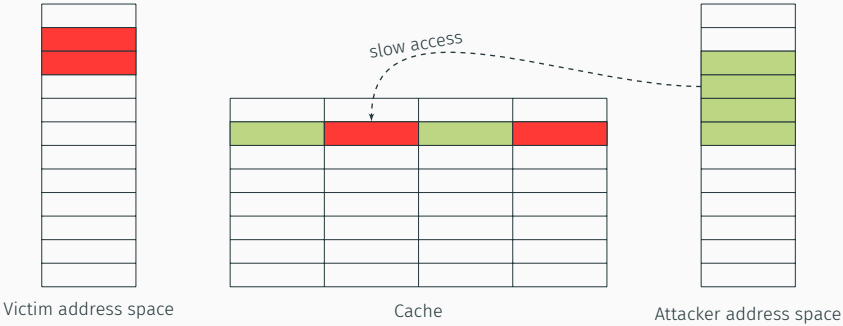
Cache attacks: Prime+Probe



Step 1: Attacker primes, *i.e.*, fills, the cache (no shared memory)

Step 2: Victim evicts cache lines while running

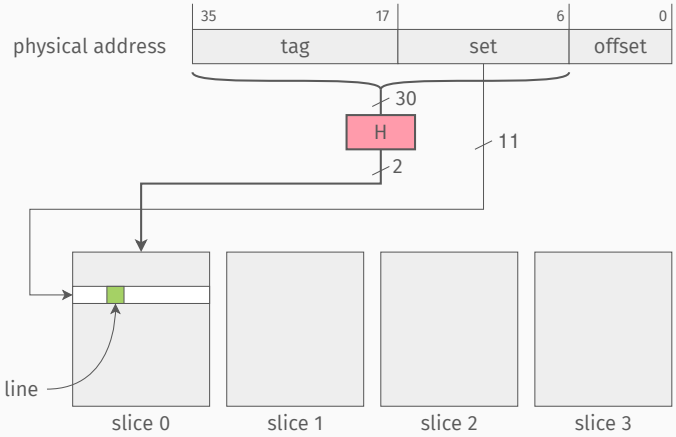
Step 3: Attacker probes data to determine if set has been accessed

Challenges with Prime+Probe

We need to evict caches lines without `clflush` or shared memory:

1. which addresses do we access to have congruent cache lines?
2. without any privilege?
3. and in which order do we access them?

Last-level cache addressing



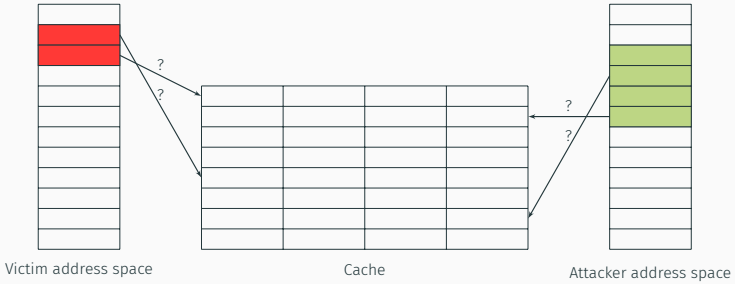
Last-level cache addressing

- last-level cache $\rightarrow$ as many slices as cores
- undocumented hash function that maps a physical address to a slice
- designed for performance

For 2^k slices:

Prime+Probe on recent procesors?

Undocumented function → impossible to target a set



C. Maurice, N. Le Scouarnec, C. Neumann, O. Heen, and A. Francillon. “Reverse Engineering Intel Complex Addressing Using Performance Counters”. In: *RAID’15*. 2015

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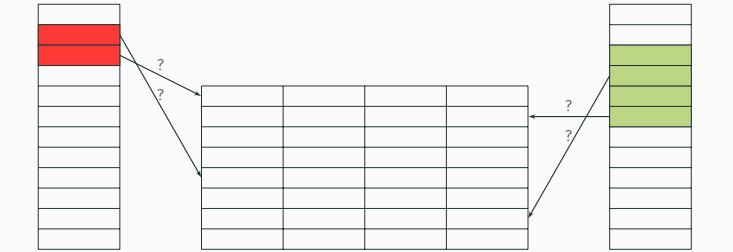

→ We reverse-engineered the function!

C. Maurice, N. Le Scouarnec, C. Neumann, O. Heen, and A. Francillon. “Reverse Engineering Intel Complex Addressing Using Performance Counters”. In: *RAID'15*. 2015

Prime+Probe: Applications

- cross-VM side channel attacks on crypto algorithms:
  - El Gamal (sliding window): full key recovery in 12 min.
- tracking user behavior in the browser, in JavaScript
- covert channels between virtual machines in the cloud

F. Liu, Y. Yarom, Q. Ge, G. Heiser, and R. B. Lee. “Last-Level Cache Side-Channel Attacks are Practical”. In: *S&P’15*. 2015.

Y. Oren, V. P. Kemerlis, S. Sethumadhavan, and A. D. Keromytis. “The Spy in the Sandbox: Practical Cache Attacks in JavaScript and their Implications”. In: *CCS’15*. 2015.

C. Maurice, M. Weber, M. Schwarz, L. Giner, D. Gruss, C. A. Boano, S. Mangard, and K. Römer. “Hello from the Other Side: SSH over Robust Cache Covert Channels in the Cloud”. In: *NDSS’17*. 2017.

Covert channels in the cloud

- covert channel: two processes communicating with each other
  - not allowed to do so, e.g., across VMs

Covert channels in the cloud

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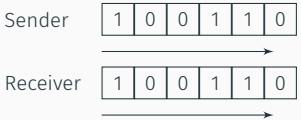
Covert channels in the cloud

- covert channel: two processes communicating with each other
  - not allowed to do so, e.g., across VMs
- literature: stops working with noise on the machine
- solution? “Just use error-correcting codes”

Why can’t we just use error correcting codes?



(a) Transmission without errors

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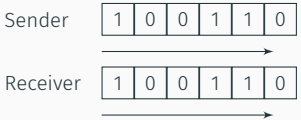

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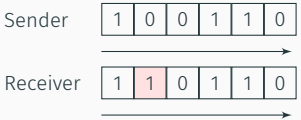

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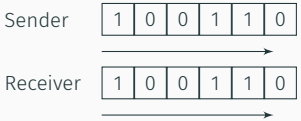

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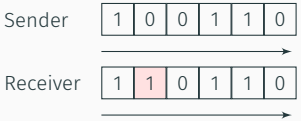
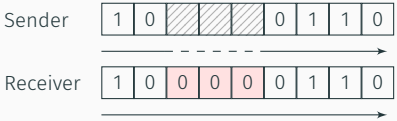


(b) Noise: substitution error



(c) Sender descheduled: insertions

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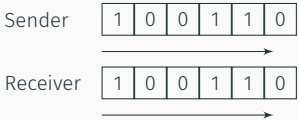

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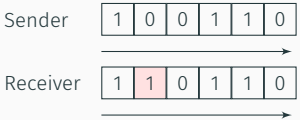

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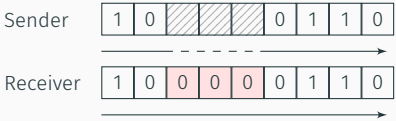

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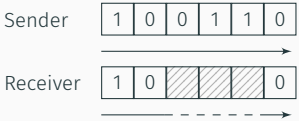

(d) Receiver descheduled: deletions

Our robust covert channel

- physical layer:
  - transmits words as a sequence of ‘0’s and ‘1’s
  - deals with synchronization errors
- data-link layer:
  - divides data to transmit into packets
  - corrects the remaining errors

Physical layer: Sending ‘0’s and ‘1’s

- sender and receiver agree on one set

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Physical layer: Sending ‘0’s and ‘1’s

- sender and receiver agree on one set
- receiver probes the set continuously
- sender transmits ’0’ doing nothing
  → lines of the receiver still in cache → fast access
- sender transmits ’1’ accessing addresses in the set
  → evicts lines of the receiver → slow access

Eviction set generation

- need a set of addresses in the same cache set and same slice

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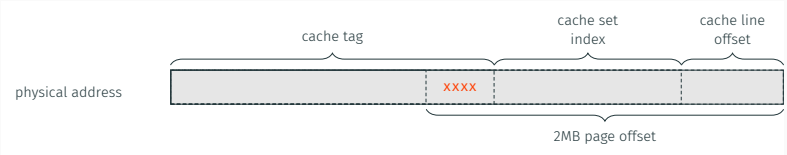

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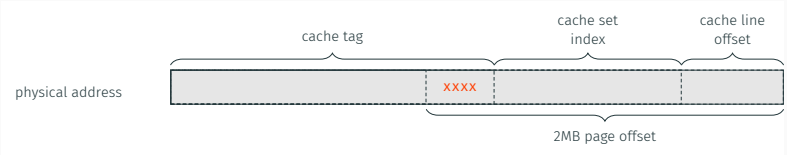
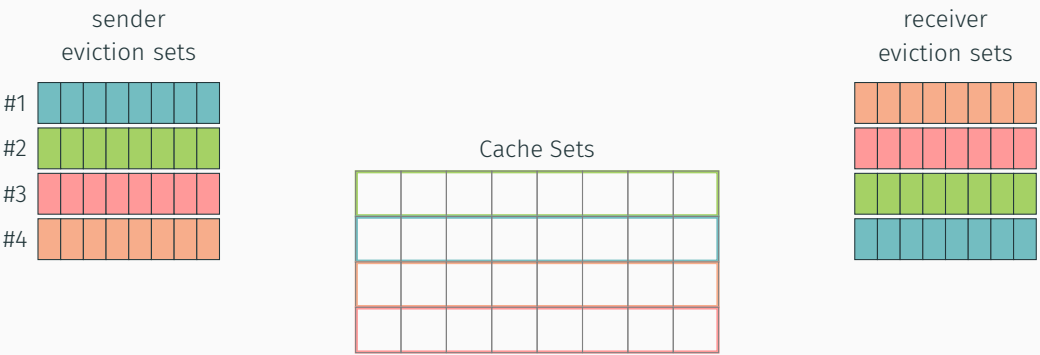


- we can build a set of addresses in the same cache set and same slice
- without knowing which slice

Jamming agreement



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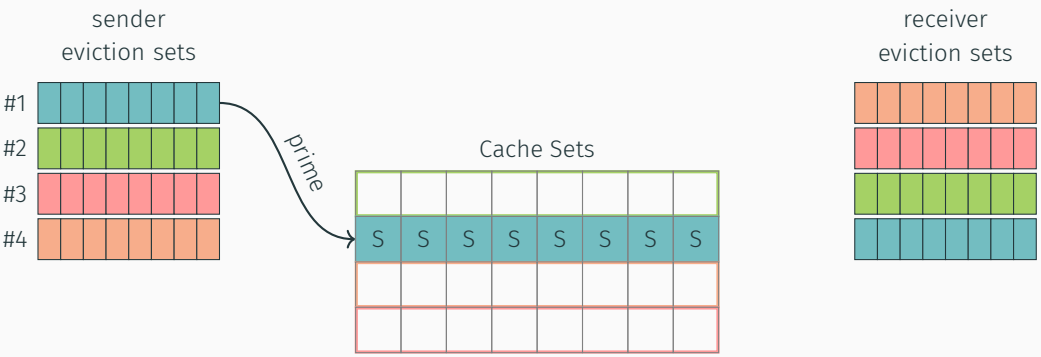

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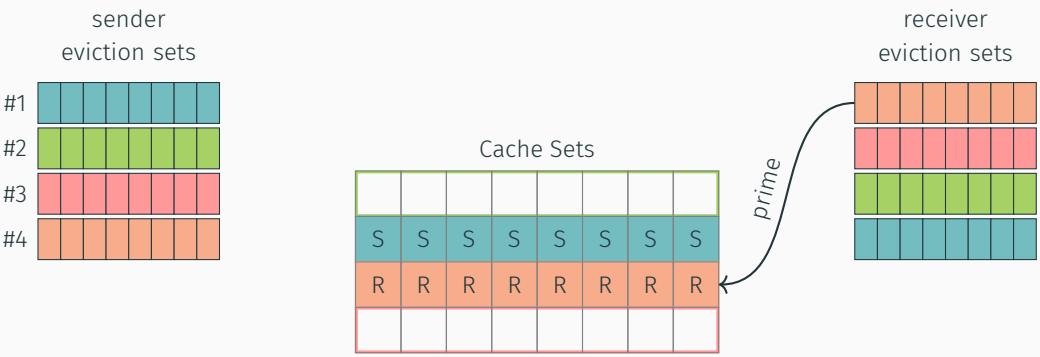

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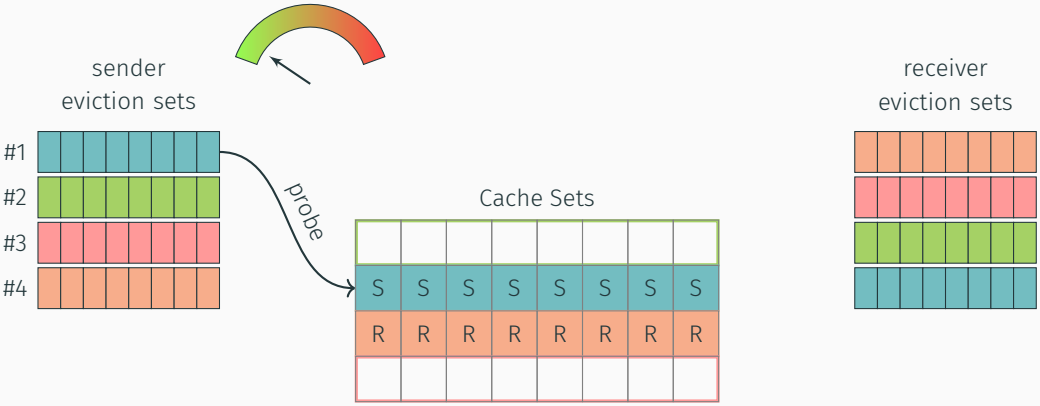

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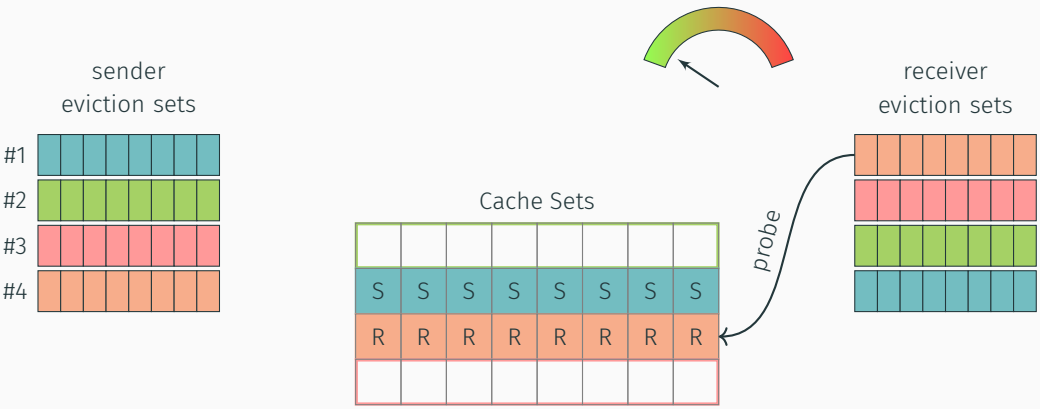

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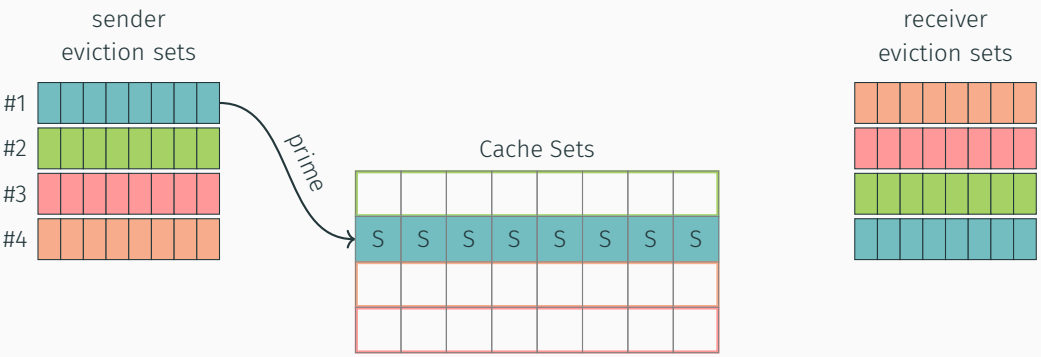

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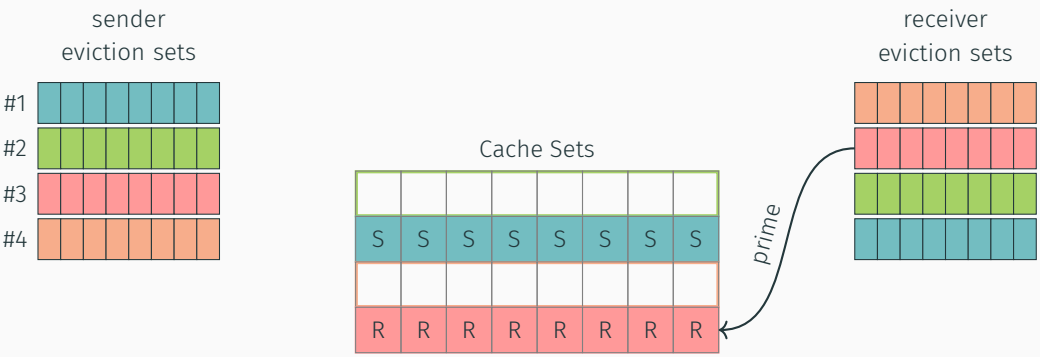

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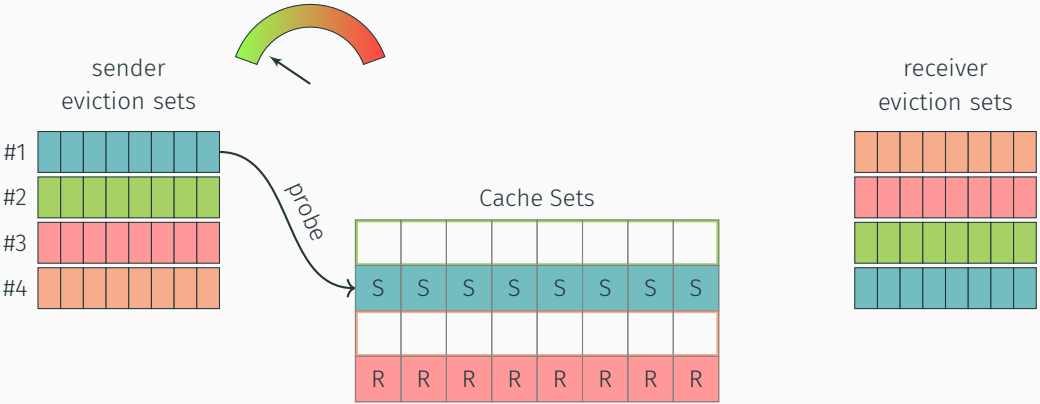

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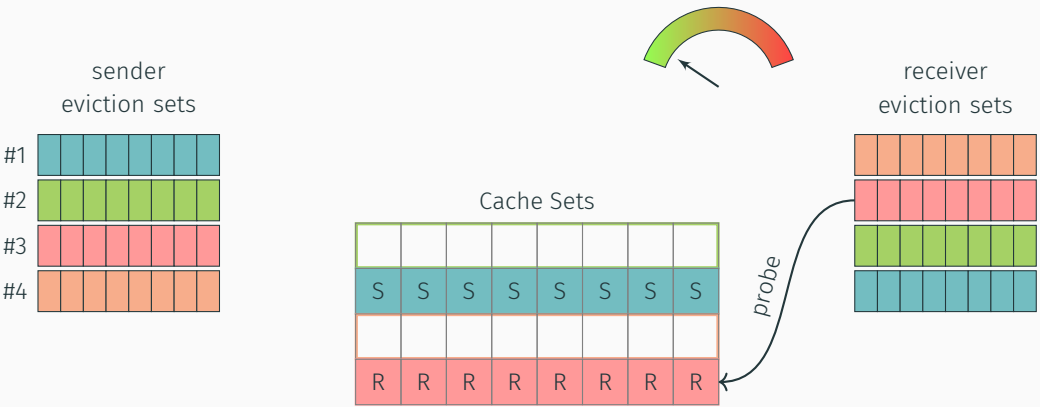

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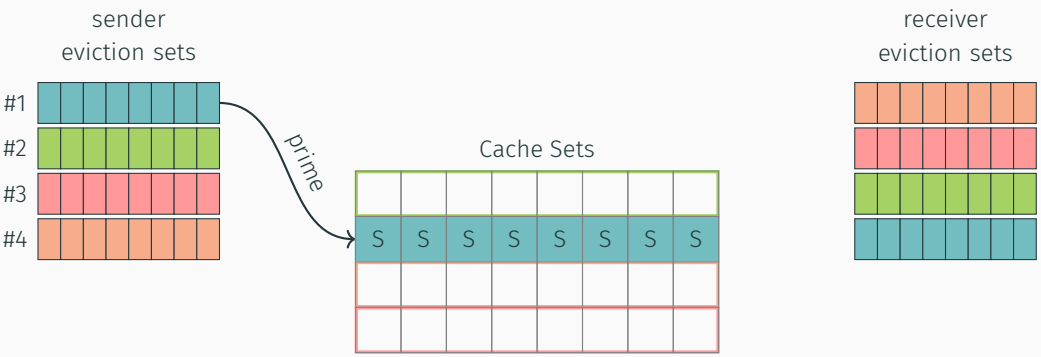

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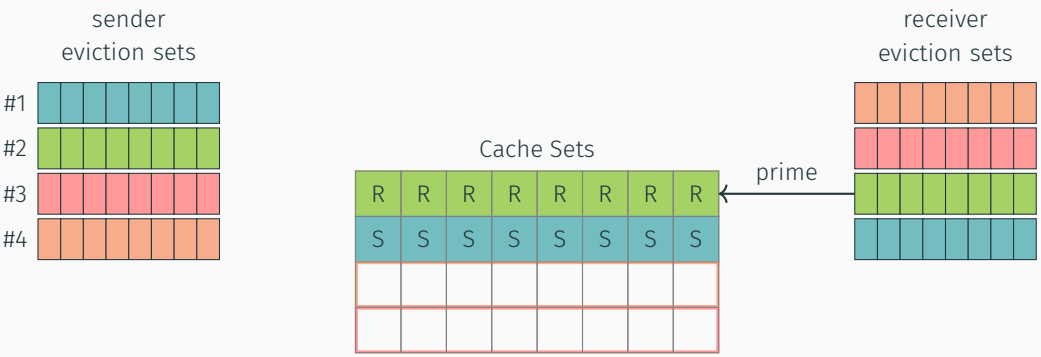

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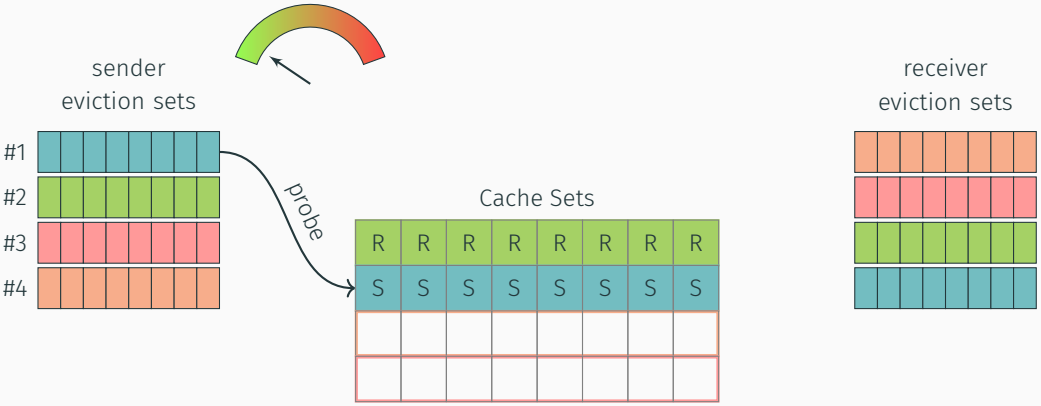

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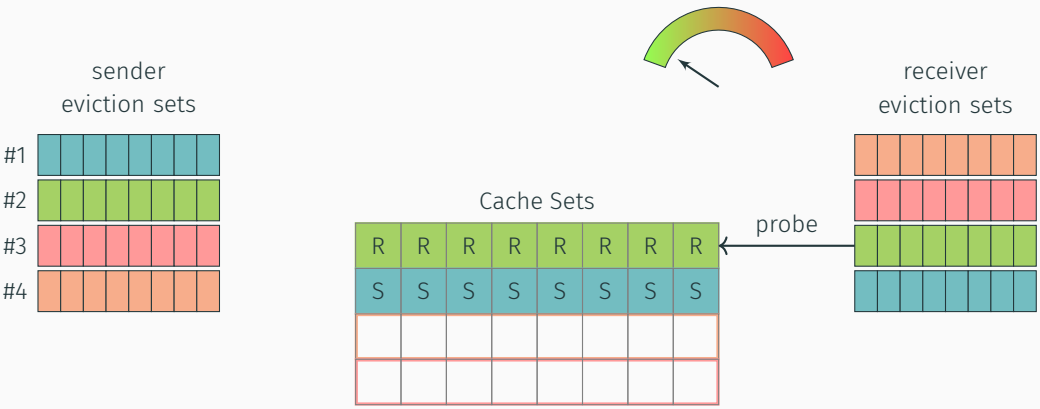

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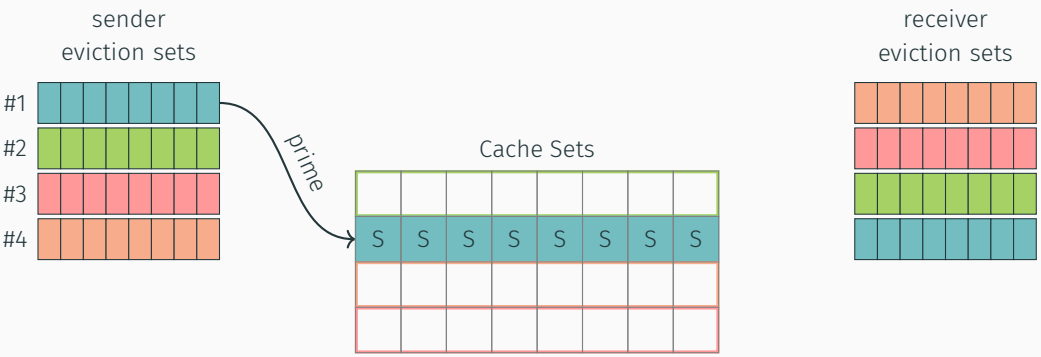

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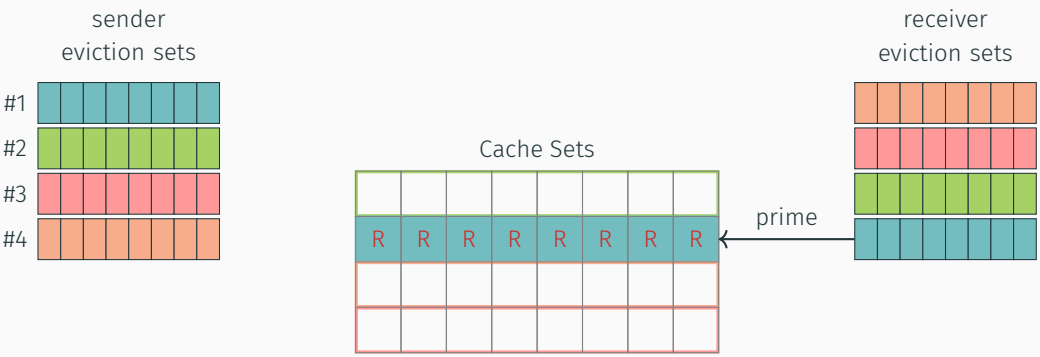

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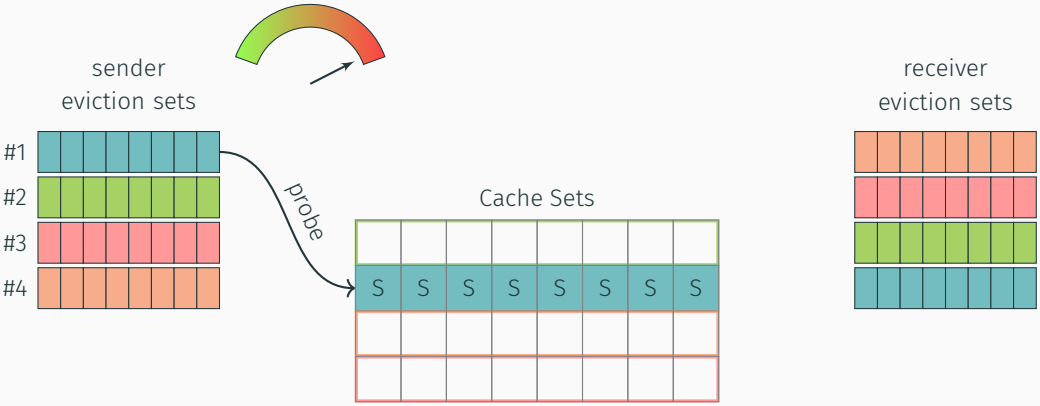

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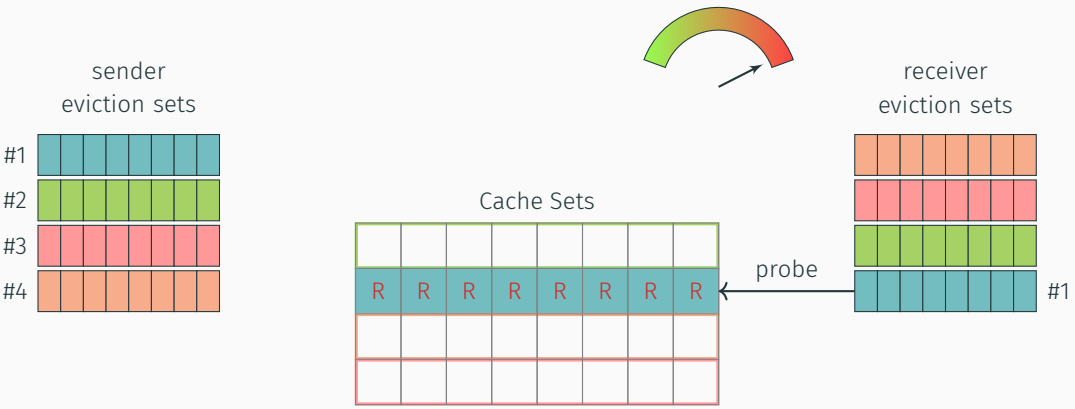

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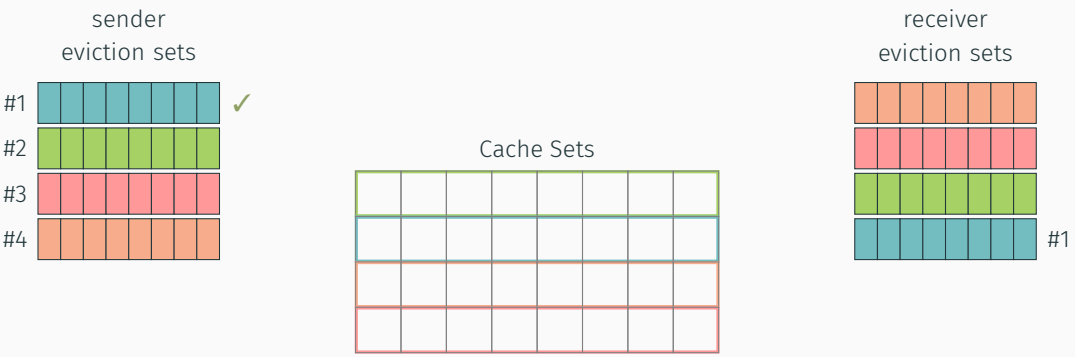

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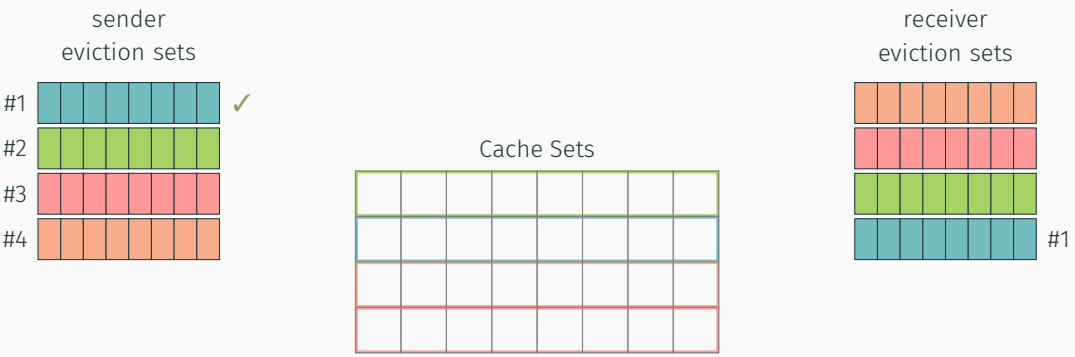

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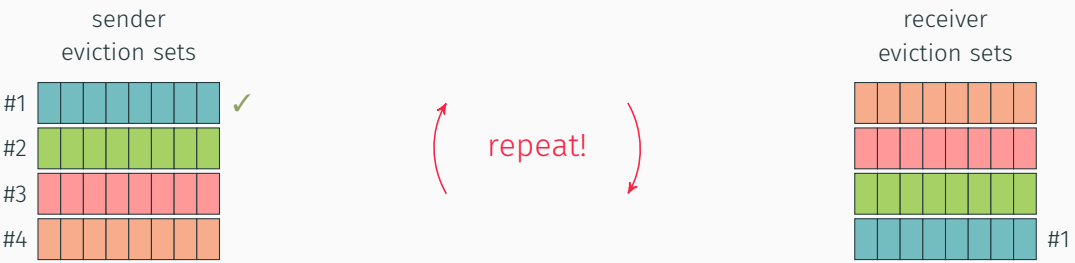

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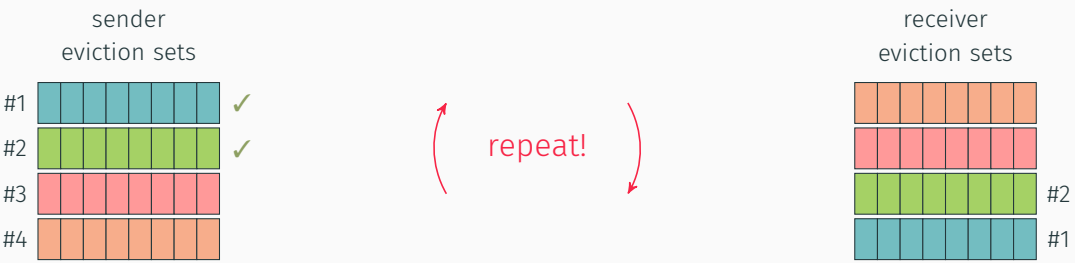

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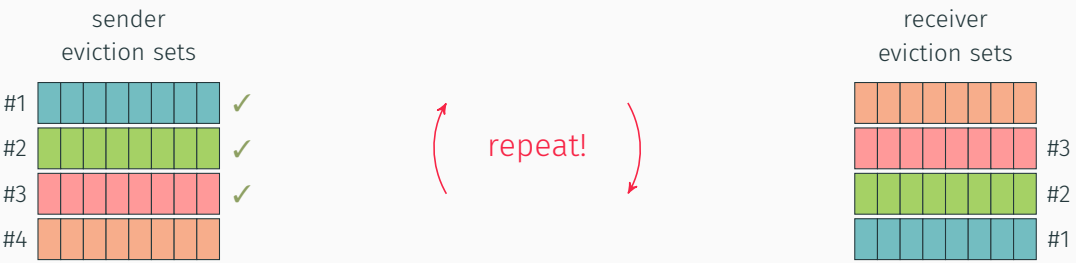

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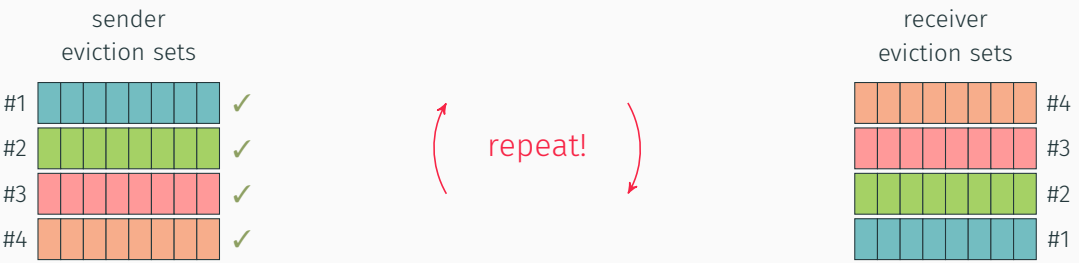
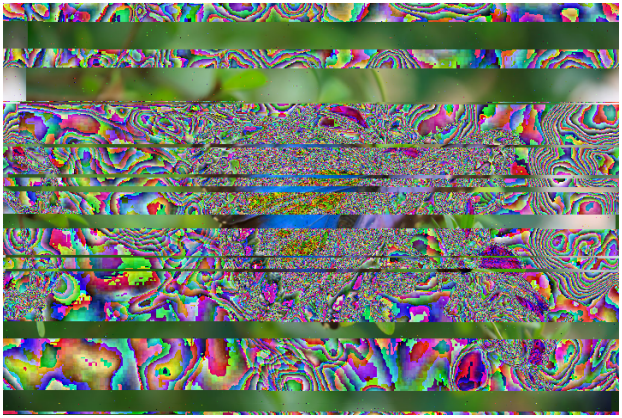


Sending the first image



Handling synchronization errors

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- deletion errors: request-to-send scheme that also serves as ack
  - 3-bit sequence number
  - request: encoded sequence number (7 bits)

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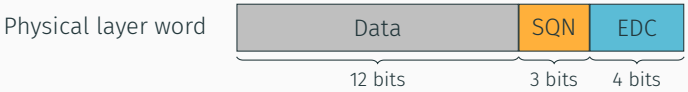
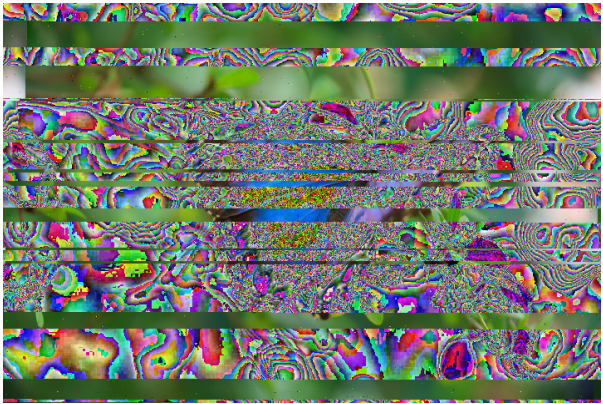
- deletion errors: request-to-send scheme that also serves as ack
  - 3-bit sequence number
  - request: encoded sequence number (7 bits)
- '0'-insertion errors: error detection code → Berger codes
  - appending the number of '0's in the word to itself

  → property: a word cannot consist solely of '0's



Synchronization (before)



Synchronization (after)

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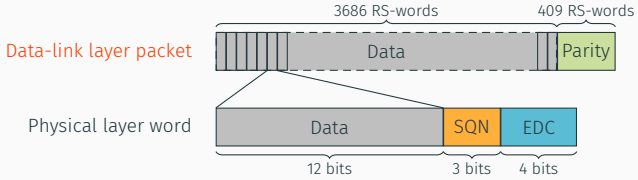
Data-link layer: Error correction

- Reed-Solomon codes to correct the remaining errors

Data-link layer: Error correction

- Reed-Solomon codes to correct the remaining errors
- RS word size = physical layer word size = 12 bits
- packet size = $2^{12} - 1 = 4095$ RS words
- 10% error-correcting code: 409 parity and 3686 data RS words



Error correction (after)

Evaluation

Environment	Bit rate	Error rate	Noise
Native	75.10 KBps	0.00%	–

Evaluation

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Native	36.03 KBps	0.00%	`stress -m 1`

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Evaluation

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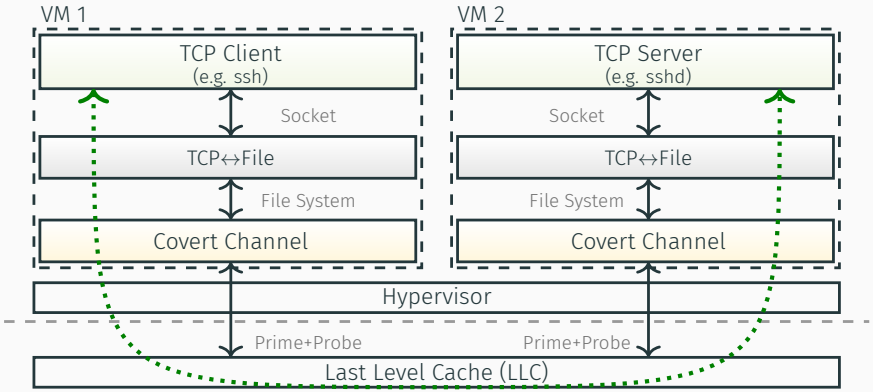
Native	36.03 KBps	0.00%	`stress -m 1`
Amazon EC2	45.25 KBps	0.00%	–
Amazon EC2	45.09 KBps	0.00%	web server serving files on sender VM
Amazon EC2	42.96 KBps	0.00%	`stress -m 2` on sender VM
Amazon EC2	42.26 KBps	0.00%	`stress -m 1` on receiver VM
Amazon EC2	37.42 KBps	0.00%	web server on all 3 VMs, `stress -m 4` on 3rd VM, `stress -m 1` on sender and receiver VMs
Amazon EC2	34.27 KBps	0.00%	`stress -m 8` on third VM

Building an SSH connection



SSH evaluation

Between two instances on Amazon EC2

Noise	Connection
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Telnet also works with occasional corrupted bytes with `stress -m 1`

Easy solution #3

Possible side channels using components shared by a CPU?

Easy solution #3

Possible side channels using components shared by a CPU?

Stop sharing a CPU!

Cross-CPU Side-Channel Attacks

What if?

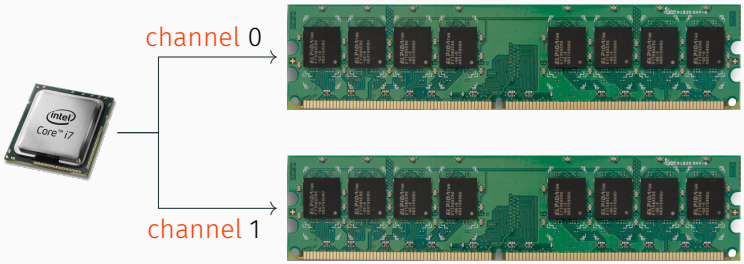
- VMs located on the same physical machine, but on separate CPUs?

What if?

- VMs located on the same physical machine, but on separate CPUs?
- they share some DRAM!

DRAM organization

DRAM organization



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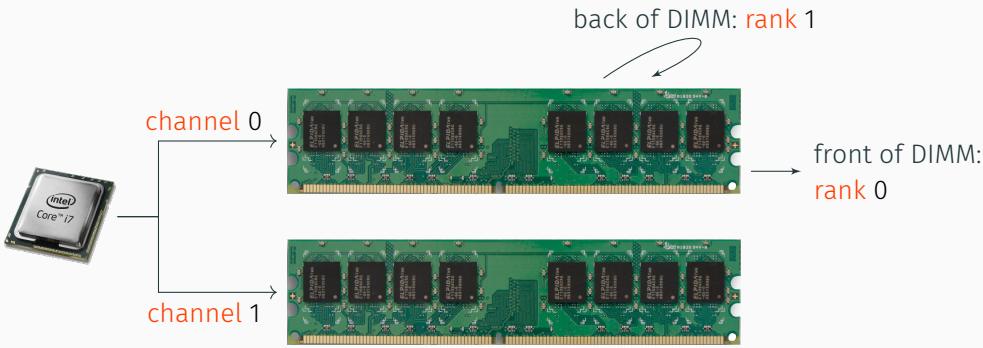

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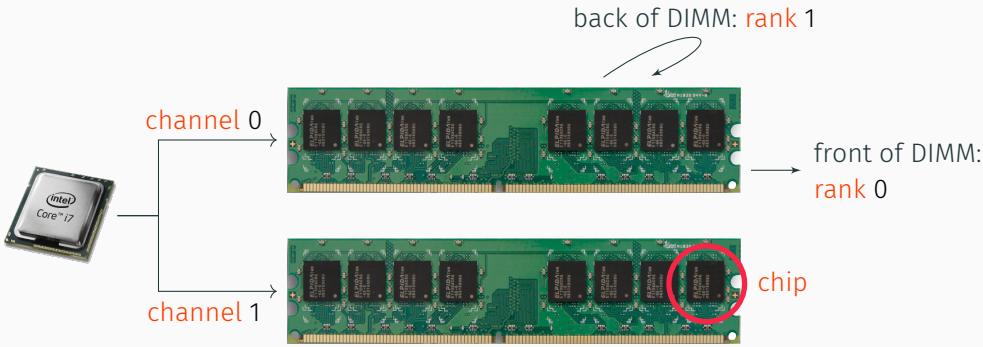
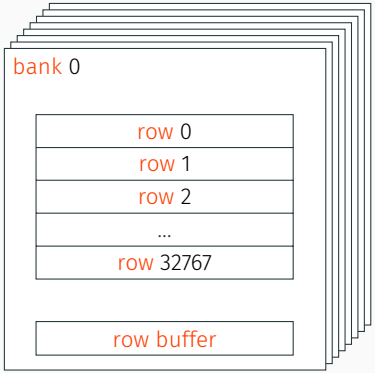


DRAM organization

chip



→ bits in cells in rows

DRAM row buffer

- DRAM internally is only capable of reading entire rows

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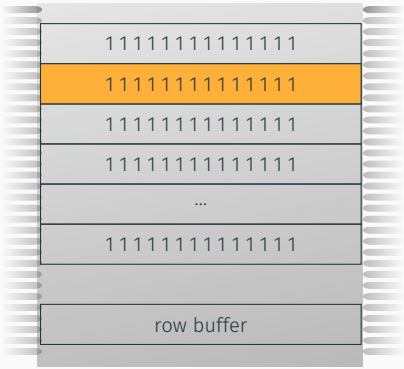
→ row buffer

How reading from DRAM works



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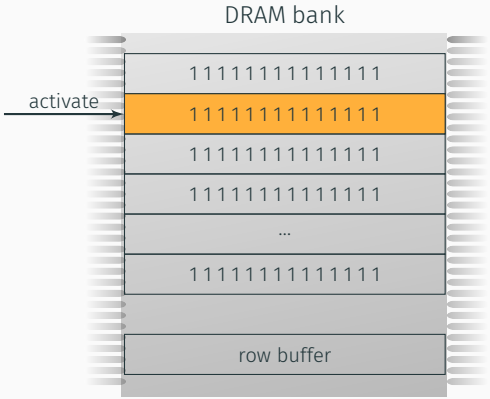

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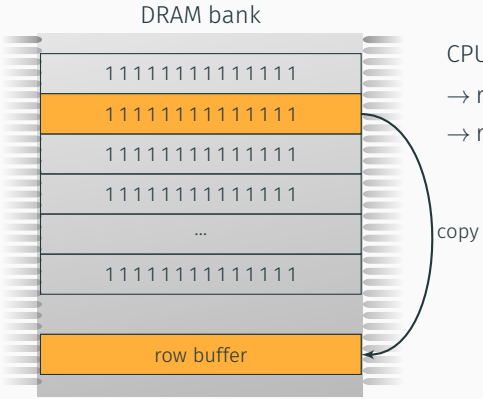

CPU wants to access row 1

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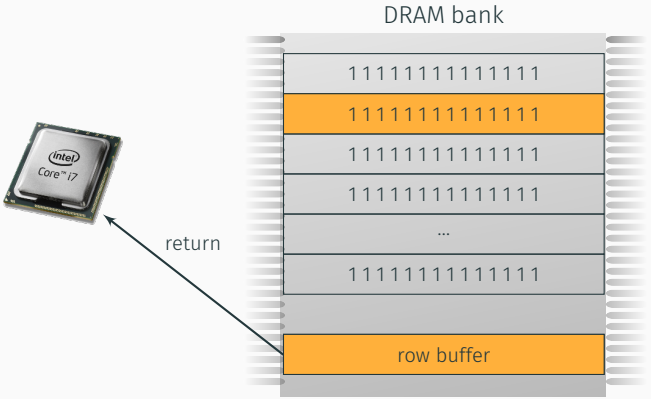

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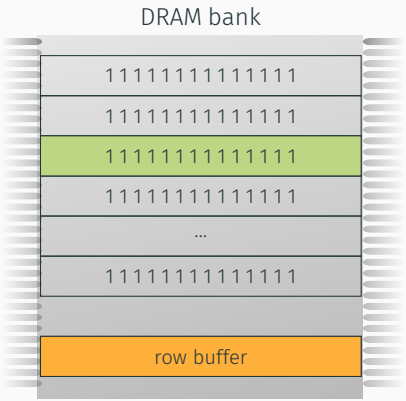

CPU wants to access row 2

How reading from DRAM works

activate

DRAM bank

1 1 1 1 1 1 1 1 1 1 1 1 1 1

1 1 1 1 1 1 1 1 1 1 1 1 1 1

1 1 1 1 1 1 1 1 1 1 1 1 1 1

1 1 1 1 1 1 1 1 1 1 1 1 1 1

...

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row buffer

CPU wants to access row 2

$\rightarrow$ row 2 activated

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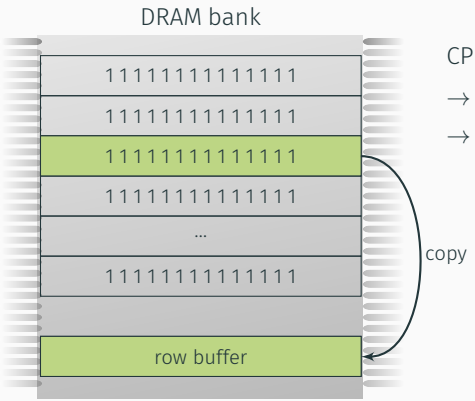

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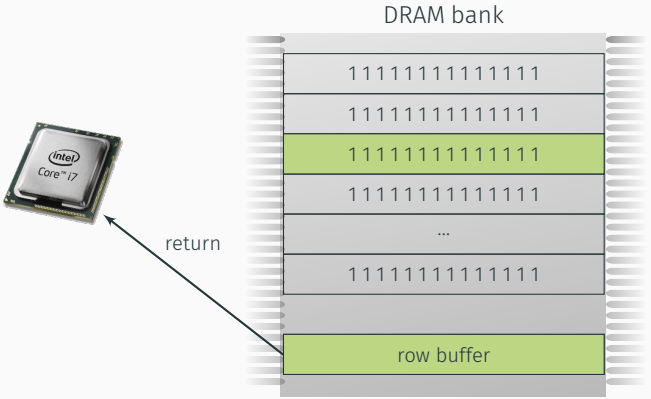

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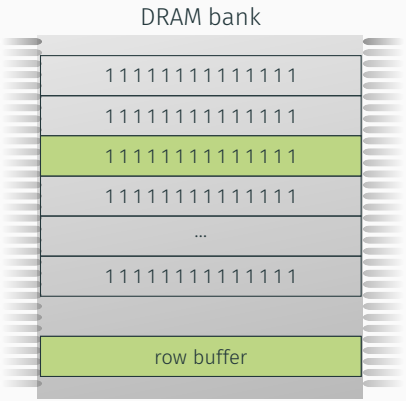


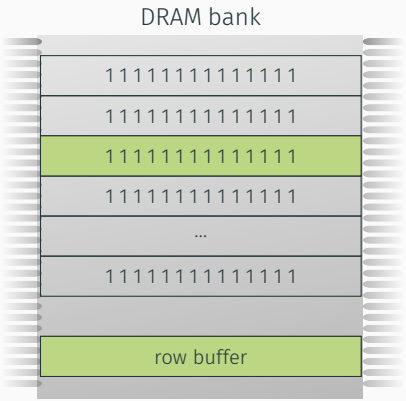
CPU wants to access row 2

→ row 2 activated

→ row 2 copied to row buffer

→ slow (row conflict)

How reading from DRAM works



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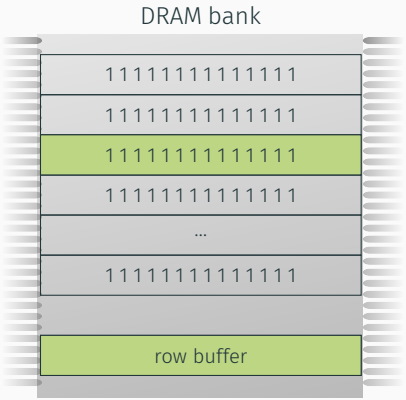

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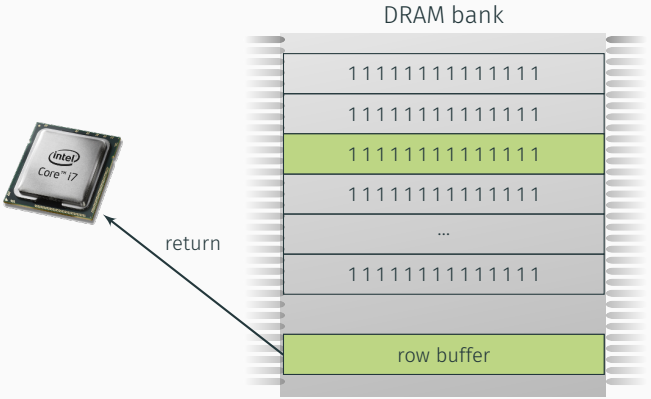

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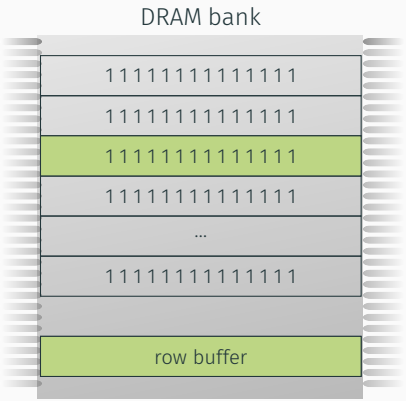

CPU wants to access row 2—again

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→ fast (row hit)

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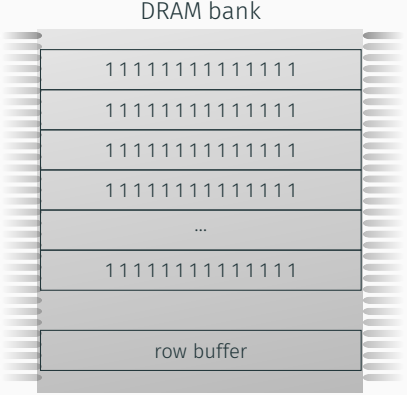
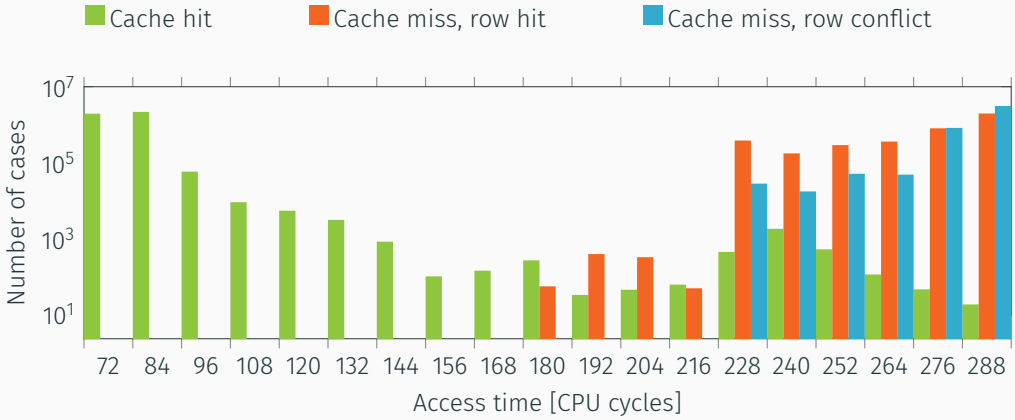


row buffer = cache

DRAM timing differences



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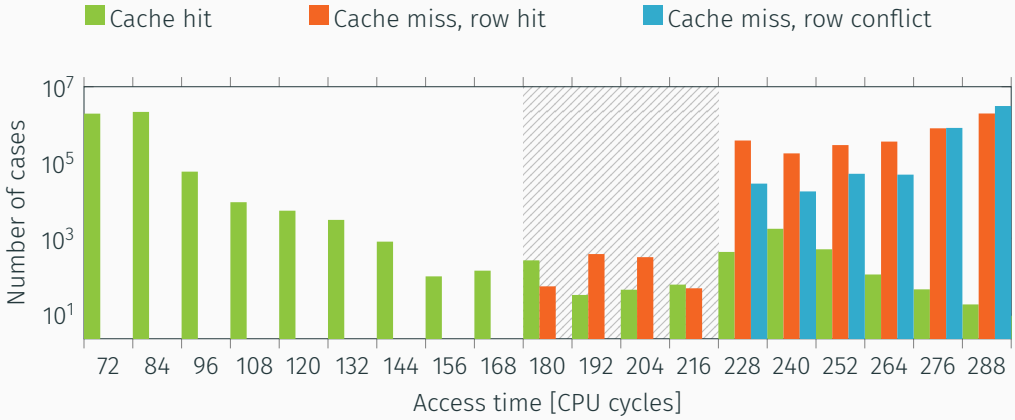

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→ we reverse-engineered them!

P. Pessl, D. Gruss, C. Maurice, M. Schwarz, and S. Mangard. “DRAMA: Exploiting DRAM Addressing for Cross-CPU Attacks”. In: *USENIX Security Symposium*. 2016

DRAMA: DRAM Addressing attacks

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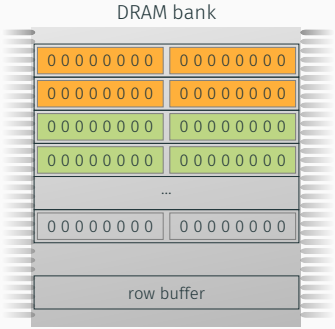
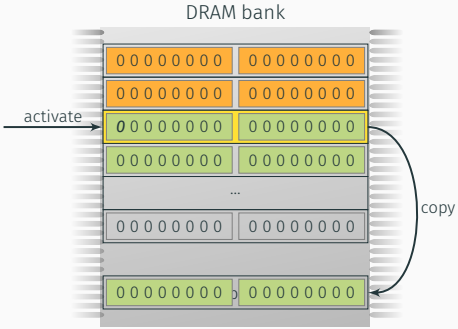
DRAMA covert channel



sender and receiver agree on one bank

receiver continuously accesses a row *i*

DRAMA covert channel



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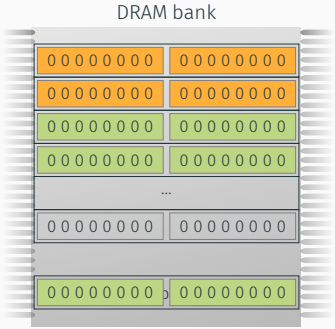

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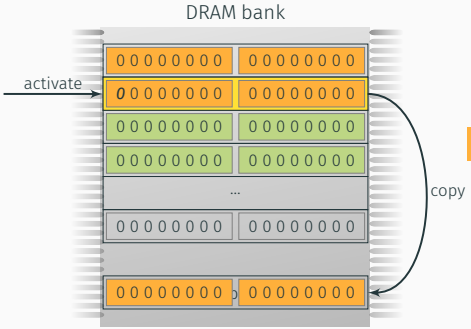

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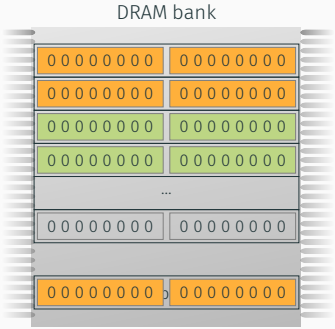

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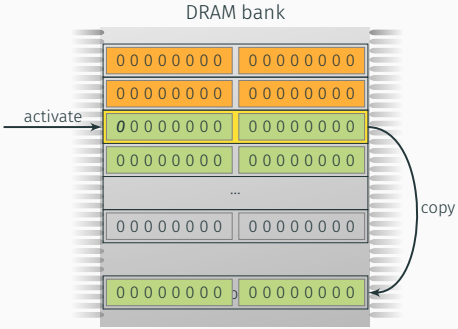

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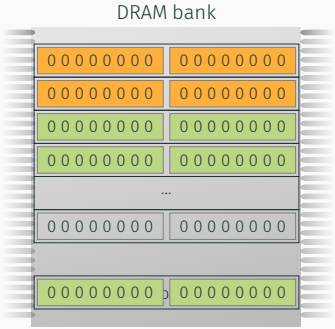

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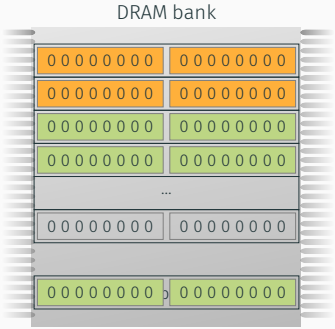

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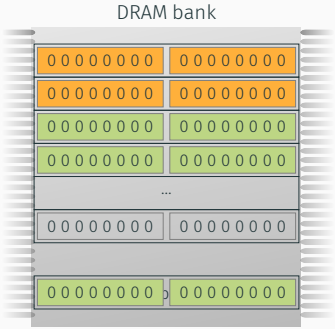

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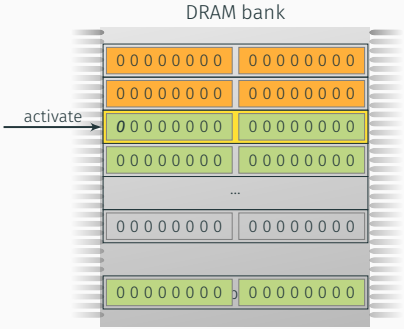

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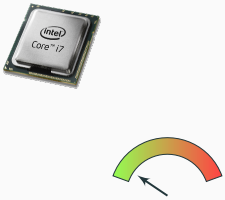

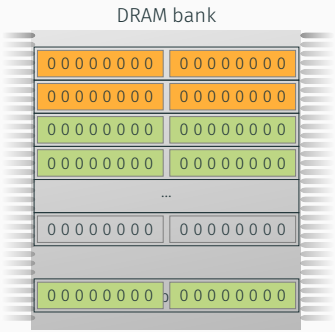

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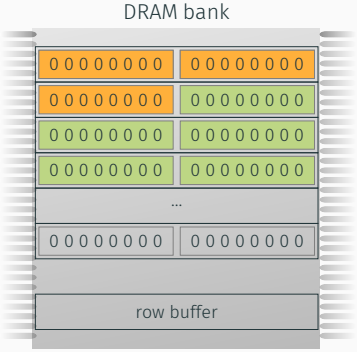
- also implemented in JavaScript
  - sender inside a VM
  - receiver runs in JavaScript in the browser on the host
  - 11 bps

DRAMA side-channel attacks



spy and victim share a row *i*

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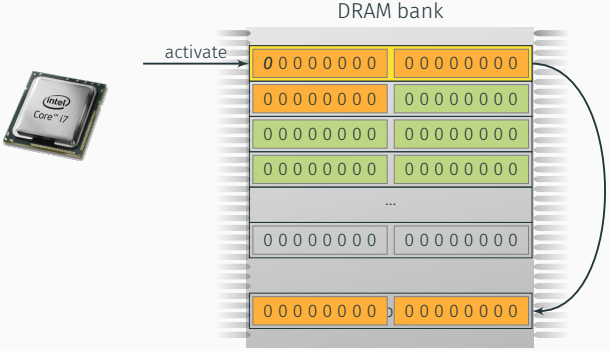

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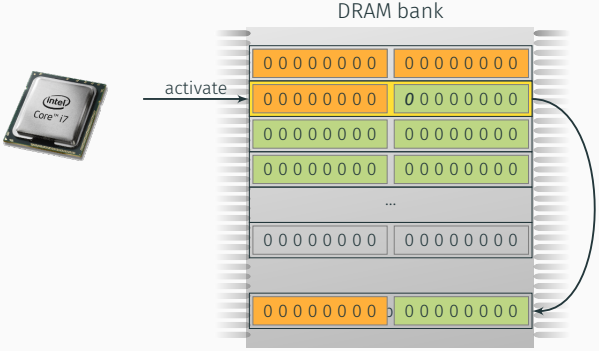

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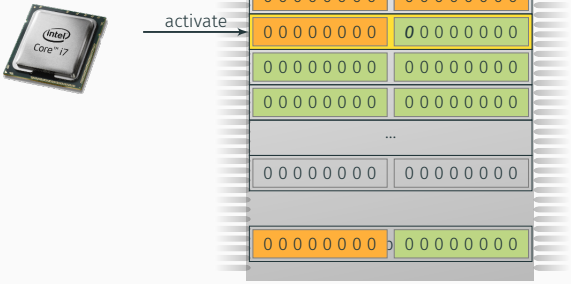

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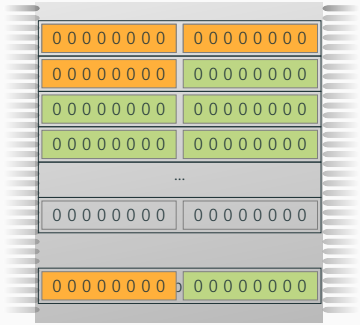
DRAMA side-channel attacks

DRAM bank



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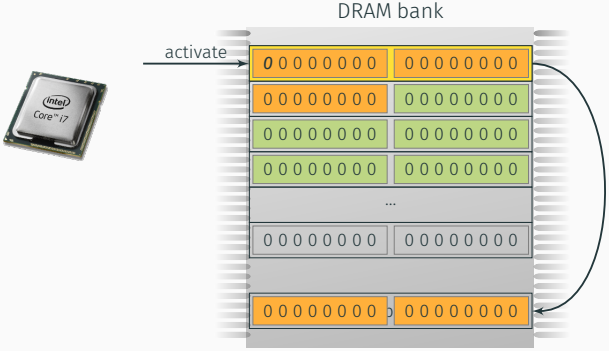

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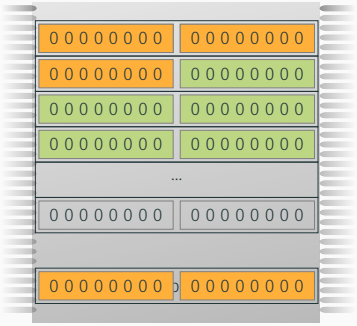

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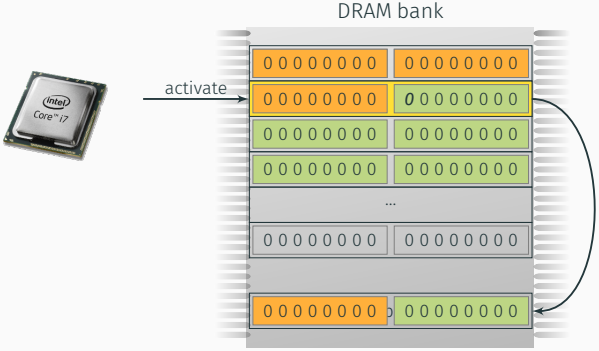

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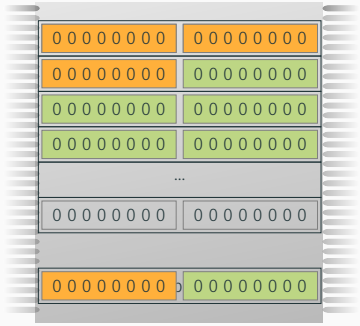

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Two related questions

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- why?

Accuracy (1)

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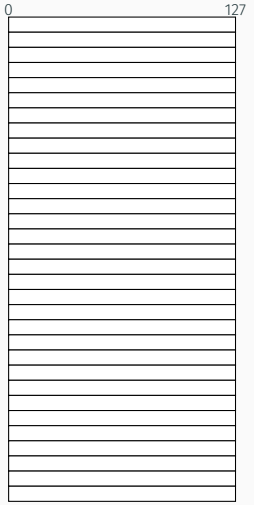
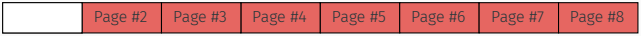
$\rightarrow$ one physical page is distributed over 4 rows

Accuracy (2)



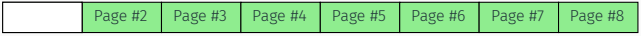
8 KB row *x* in BG0 (1) and channel (1)

8 KB row *x* in BG0 (0) and channel (1)

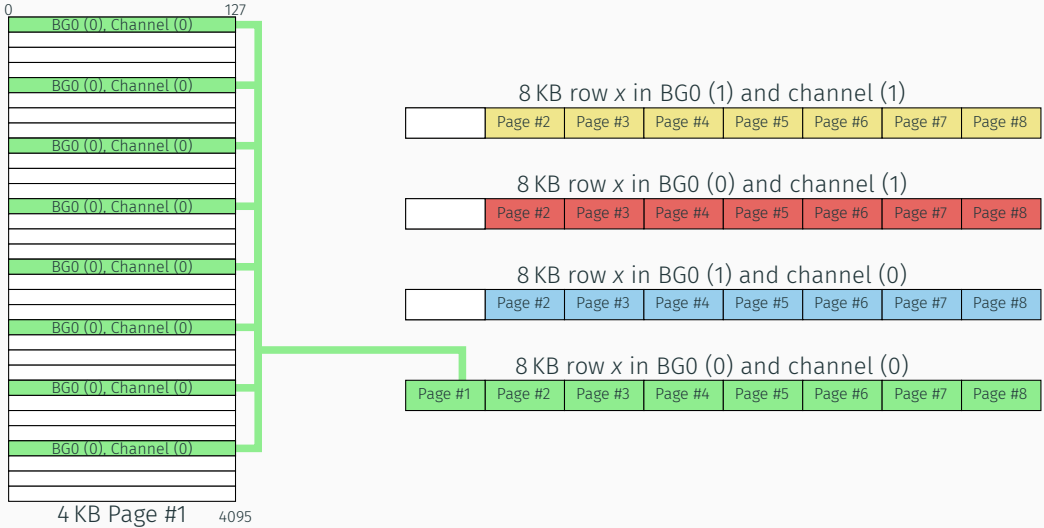


8 KB row *x* in BG0 (1) and channel (0)

8 KB row *x* in BG0 (0) and channel (0)



Accuracy (2)


0
127
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
BG0 (0), Channel (0)
4 KB Page #1
4095
8 KB row x in BG0 (1) and channel (1)
Page #2
Page #3
Page #4
Page #5
Page #6
Page #7
Page #8
8 KB row x in BG0 (0) and channel (1)
Page #2
Page #3
Page #4
Page #5
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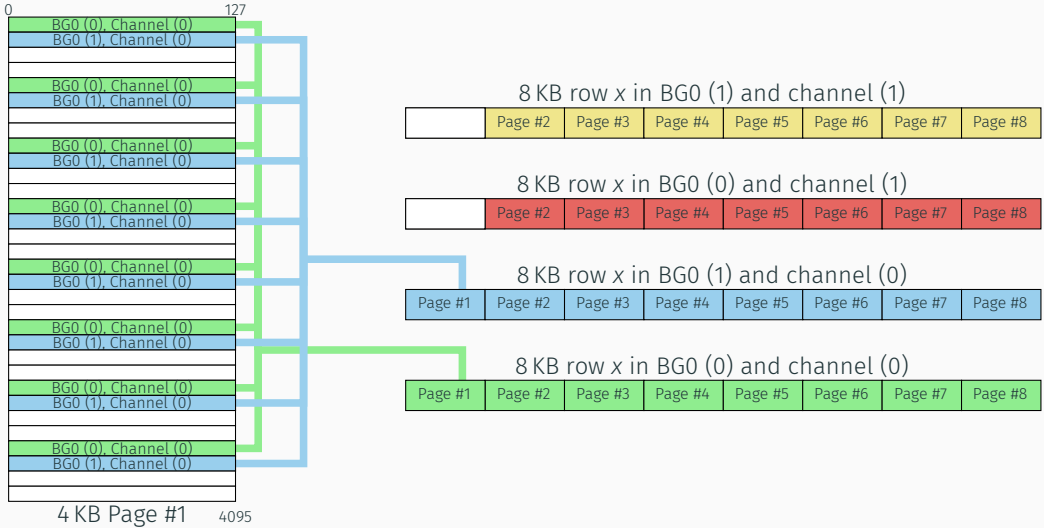
0
127
BG0 (0), Channel (0)
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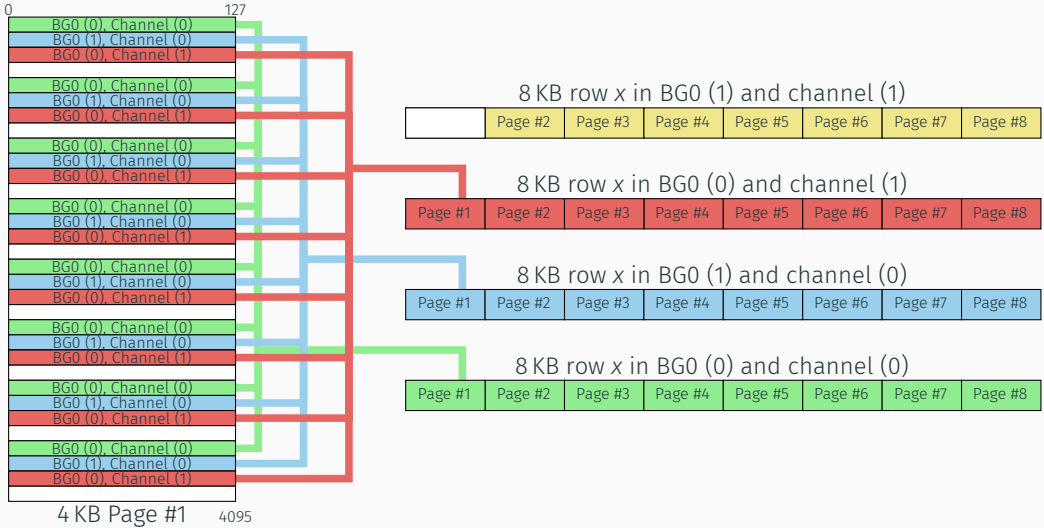
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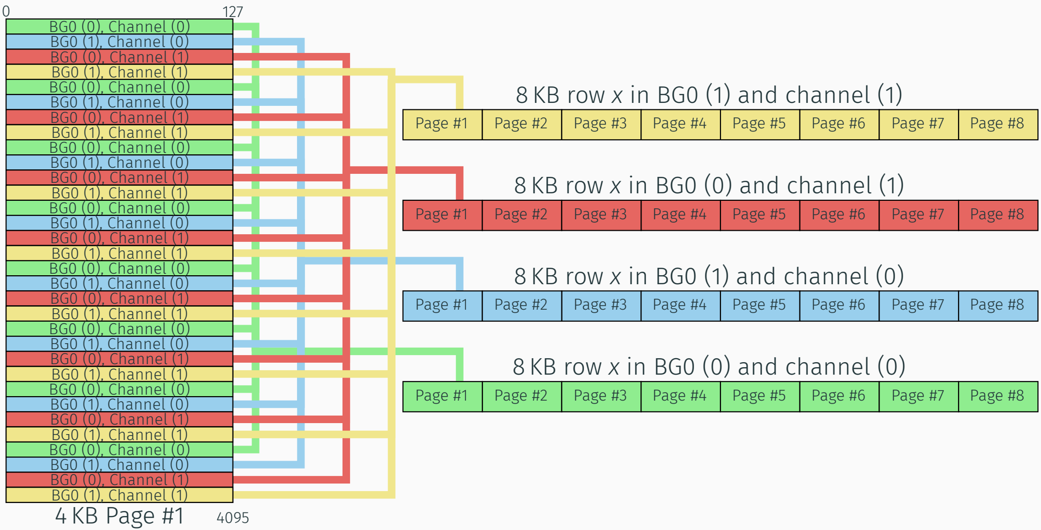
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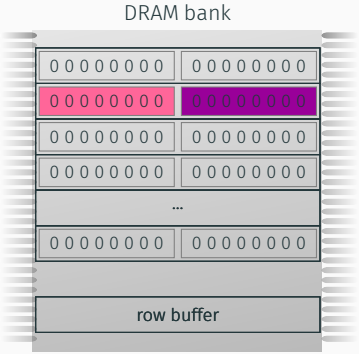
Accuracy (3)

Number of pages per row depends on DRAM configuration and CPU architecture

Sandy Bridge /w 1 DIMM



Sandy Bridge /w 1 DIMM

→ 2 pages per row

Accuracy (3)

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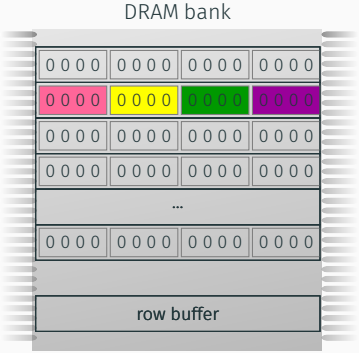
Ivy Bridge /w 2 DIMM



Sandy Bridge /w 1 DIMM

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Ivy Bridge /w 2 DIMM

→ 4 pages per row

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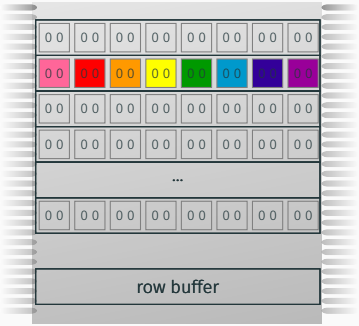
Skylake /w 2 DIMM

DRAM bank



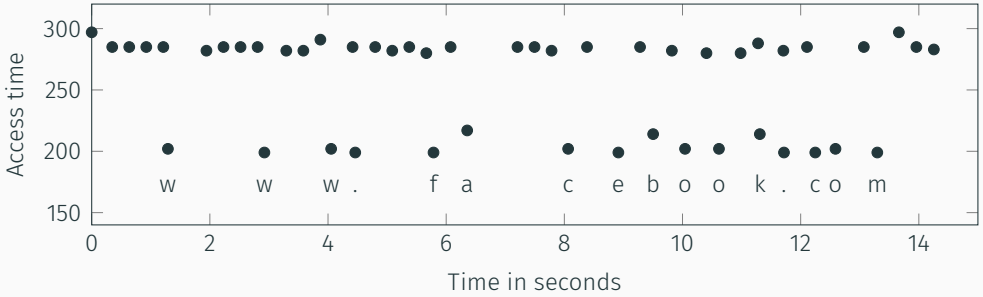
Sandy Bridge /w 1 DIMM
→ 2 pages per row

Ivy Bridge /w 2 DIMM
→ 4 pages per row

Skylake /w 2 DIMM
→ 8 pages per row

Spying on keystrokes

- side-channel: template attack
  - allocate a large fraction of memory to be in a row with the victim
  - profile memory and record row-hit ratio for each address



Easy solution #4

Possible side channels using components shared by a machine?

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Now what?

There’s more!

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Sharing hardware does not only happen in the cloud

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- JavaScript is essentially code execution

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- and between SGX enclaves

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How to counter attacks based on hardware optimizations without decreasing performance brought by these optimizations?

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Conclusion

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http://cs.adelaide.edu.au/~yval/Mastik/

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- hard to patch → issues linked to performance optimizations
- quick fixes don't work
- more work needed before having satisfying solutions

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Thank you!

Contact

- clementine@cmaurice.fr
- @BloodyTangerine

Microarchitectural Attacks in the Cloud

Clémentine Maurice

April 23, 2017—Workshop on Security and Dependability of Multi-Domain Infrastructures, Belgrade, Serbia