Flush+Flush: A Fast and Stealthy Cache Attack

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Motivations

- cache side channels are stealthy attacks $\rightarrow$ not detected by IDS

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- cache side channels are stealthy attacks → not detected by IDS
- but cache attacks have a large impact on the cache

→ use performance counters for detection [HF15; Pay16]

→ detect abnormal behavior

Contributions

- novel attack Flush+Flush
  - stealthier than previous cache attacks
  - faster than previous cache attacks
- framework to evaluate cache attacks
  - in terms of performance and detectability

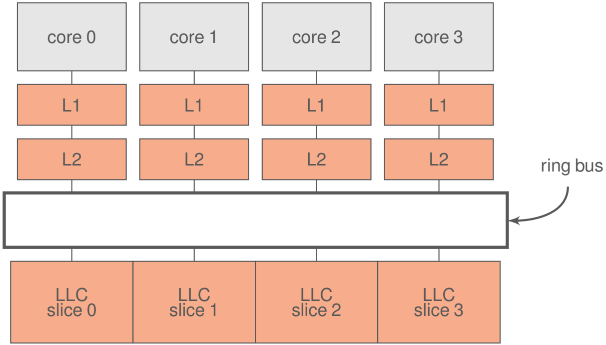
→ `https://github.com/IAIK/flush_flush`

1. Introduction

2. Flush+Flush

3. Conclusion and future work

Caches on Intel CPUs



- L1 and L2 are private
- last-level cache
  - divided in slices
  - shared across cores
  - inclusive
  - hash function for addressing [MLSNHF15]

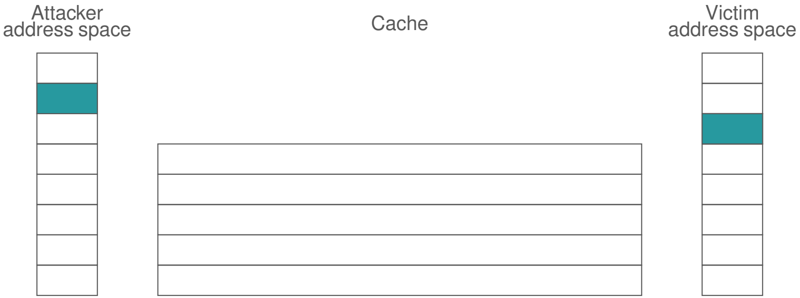
Access-driven cache attacks

Attacker monitors its own activity to find sets accessed by victim.

Flush+Reload	Prime+Probe
[GBK11]	[Per05]
[YF14]	[LYGHL15]
[GSM15]	[MNHF15]

Exploit timing difference between cache hits and cache misses

Flush+Reload



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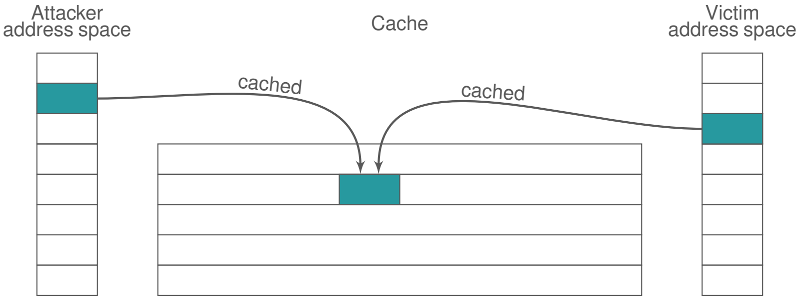

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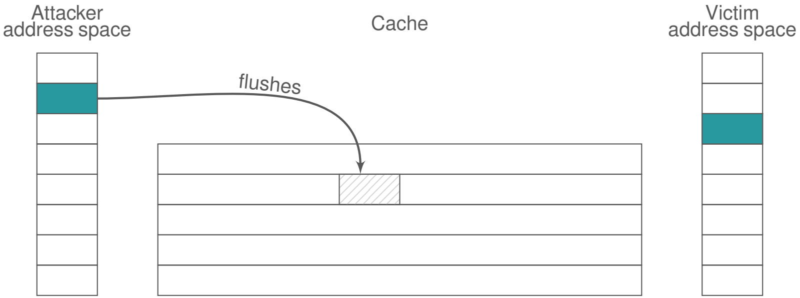

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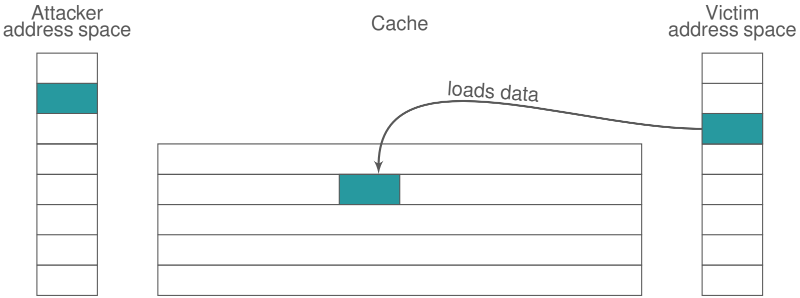

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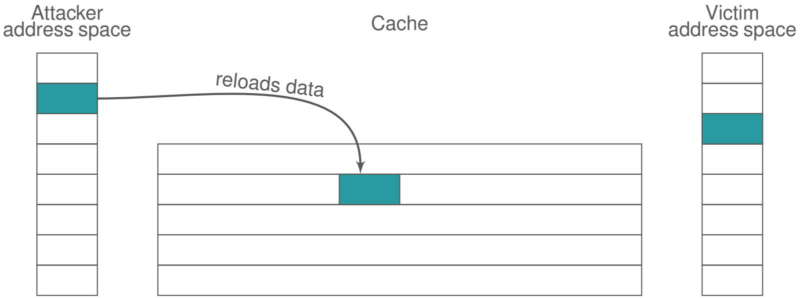

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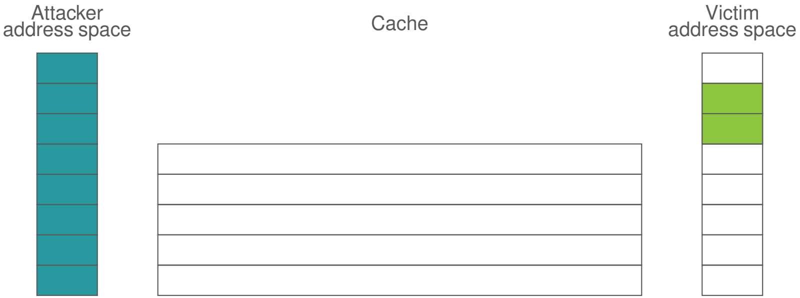
step 3: attacker reloads data → fast access if the victim loaded the line

Prime+Probe



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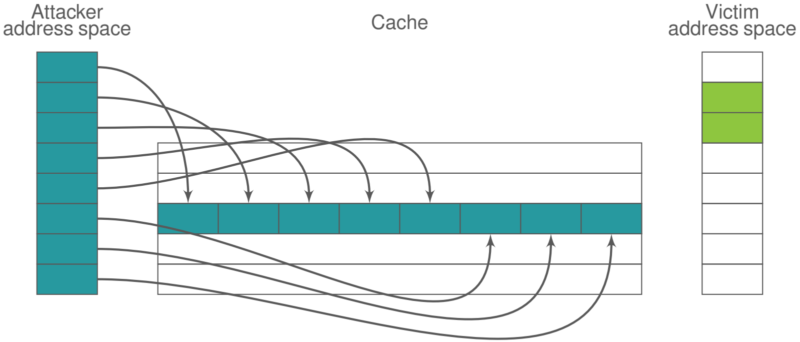

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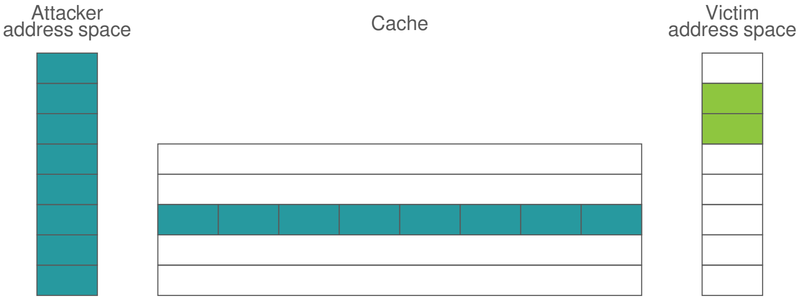

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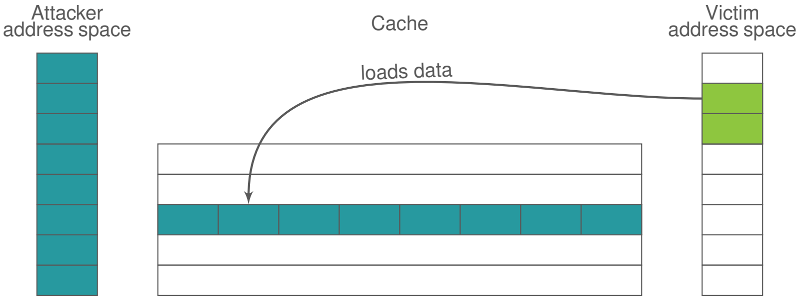

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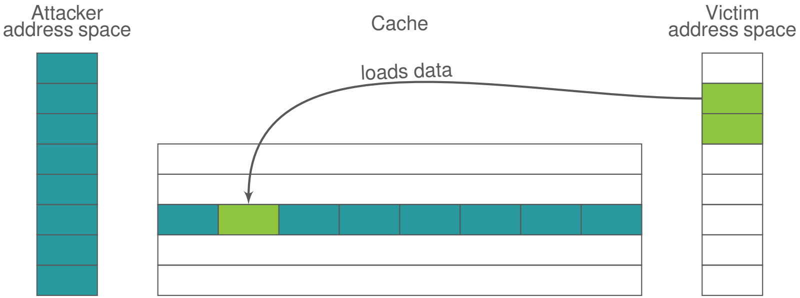

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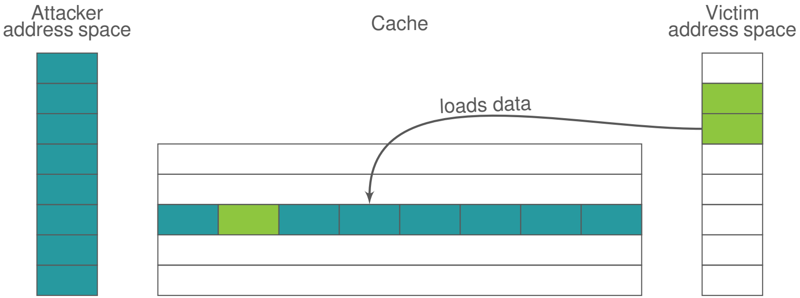

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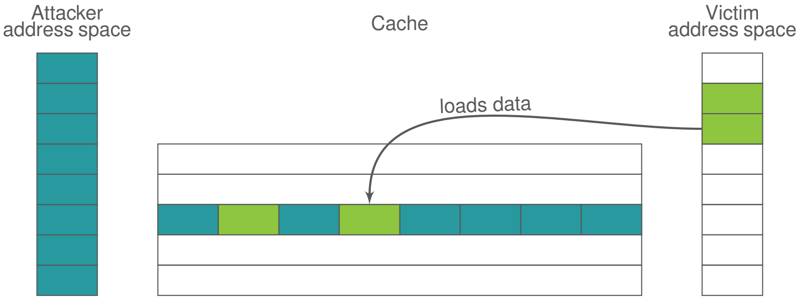

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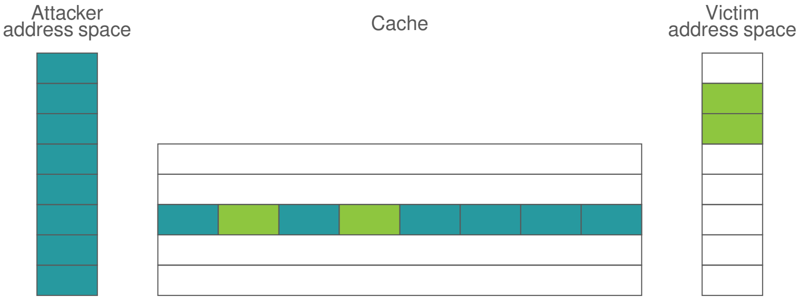

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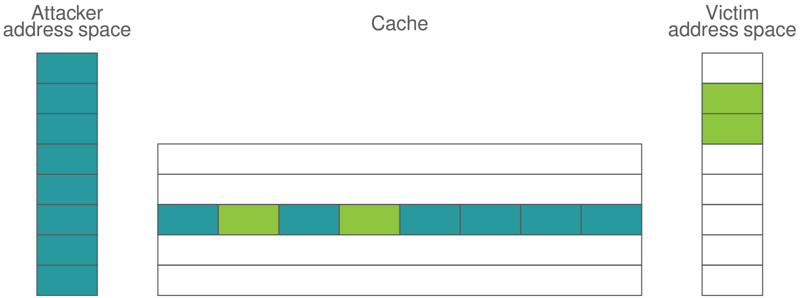

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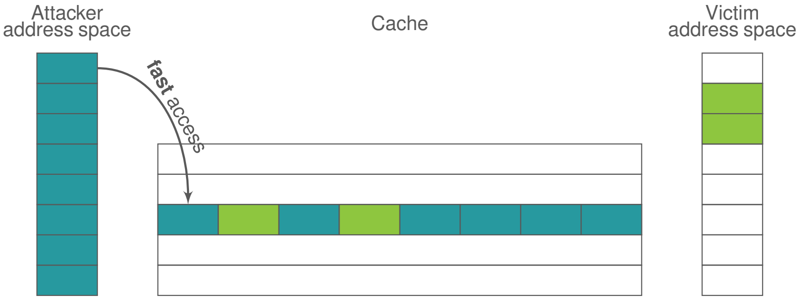

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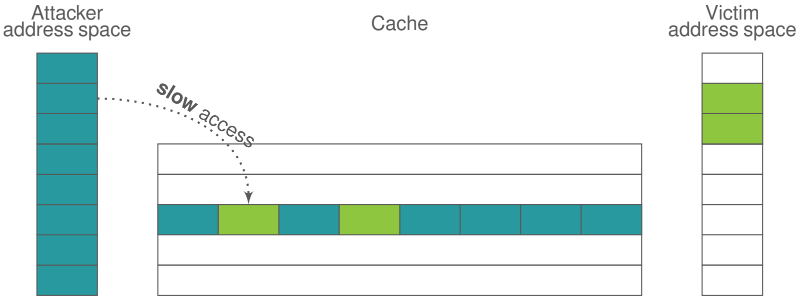

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Examples of cache attacks

Covert channel:

- cross-VM, cross-core: 600kbps [LYGHL15]

Side channel:

- cross-VM, cross-core side-channel attacks on crypto algorithms
  - RSA: 96.7% of key bits in 1 signature [YF14]
- tracking user behavior in the browser, in JavaScript [OKSK15]

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Which performance counters (1)

We analyzed events w.r.t cache attacks and benign programs:

- 23 hardware and cache performance events with `perf_event_open`
- `UNC_CBO_CACHE_LOOKUP` of CBo with MSRs

→ rmq: only possible to monitor 4 events simultaneously

Which performance counters (2)

Detecting cache attacks and Rowhammer

1. `CACHE_MISSES` → occur after data is flushed
2. `CACHE_REFERENCES` → occur when reaccessing memory
3. `L1D_RM` → occur after data is flushed
4. `LL_RA` → occur when reaccessing memory

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Detecting cache attacks and Rowhammer without false positives

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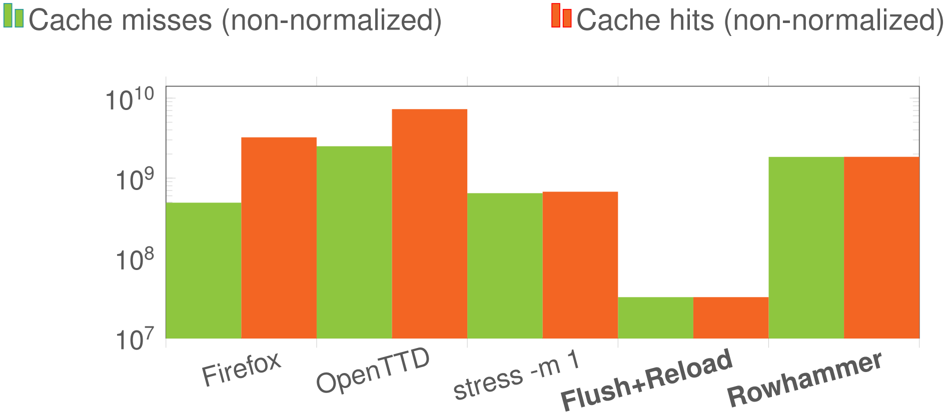
→ normalize the events by `ITLB_RA+ITLB_RM`

Detection, non-normalized



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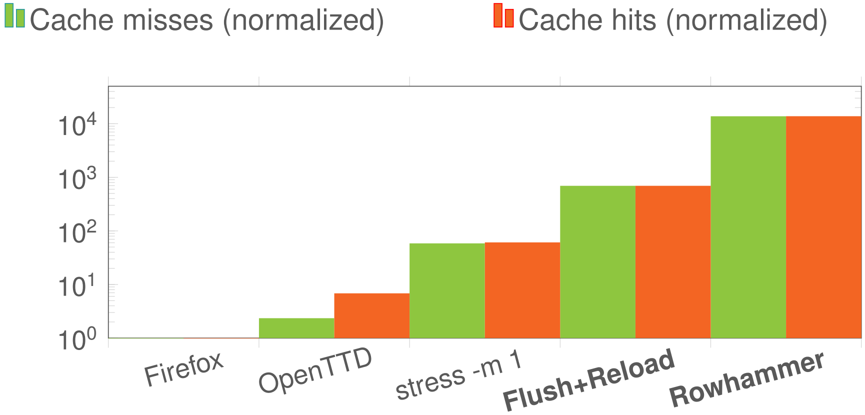

Stealthier cache attack: Flush+Flush

- motivation: detecting cache attacks with perf counters is not enough

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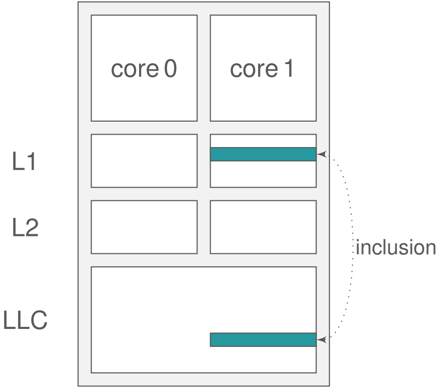
→ Flush+Flush: new cache attack, based on `clflush` timing leakage

  → stealthier than Prime+Probe and Flush+Reload
  → faster than Prime+Probe and Flush+Reload

`clflush` timing leakage (1)



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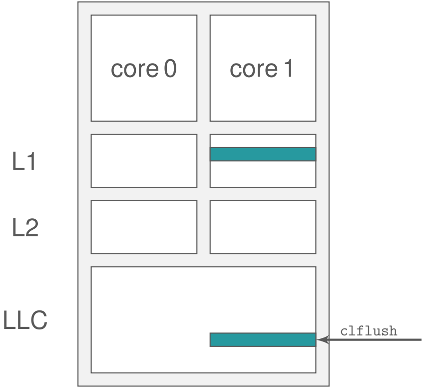

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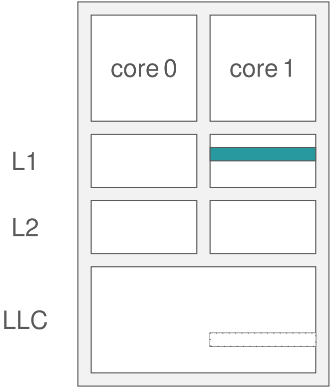

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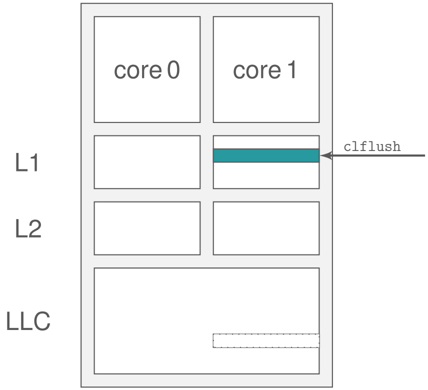

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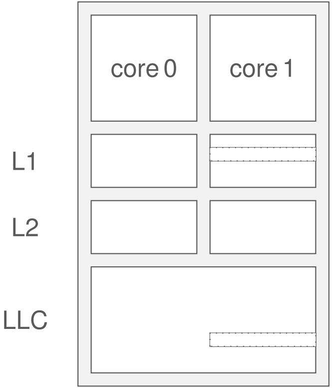

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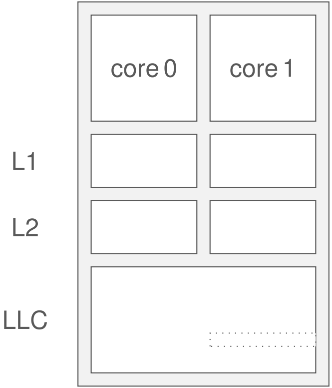

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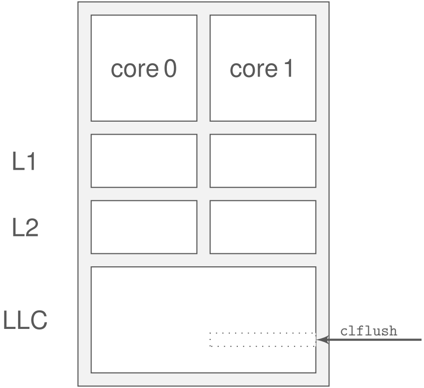

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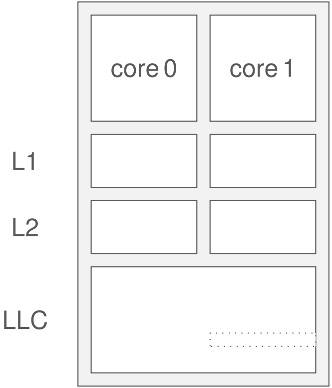

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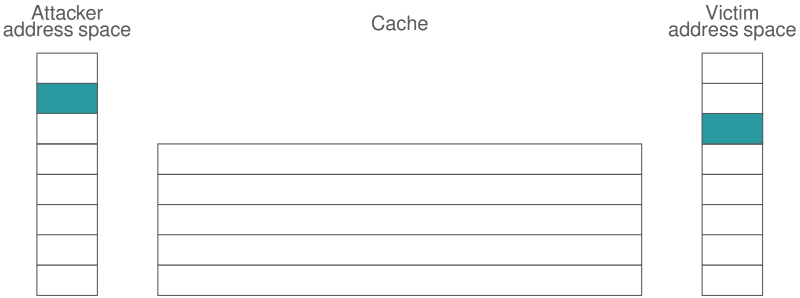
  - goes to LLC, does nothing

  → fast

`clflush` timing leakage (2)

Flush+Flush



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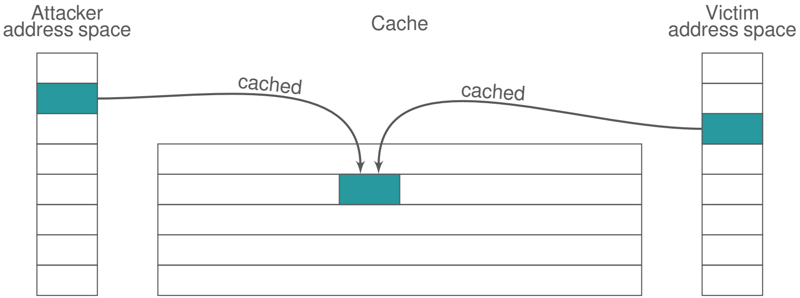

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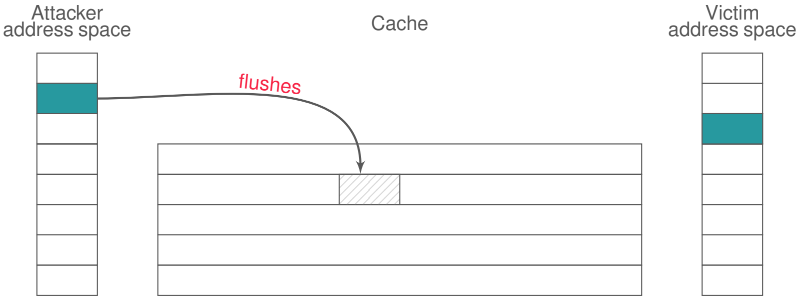

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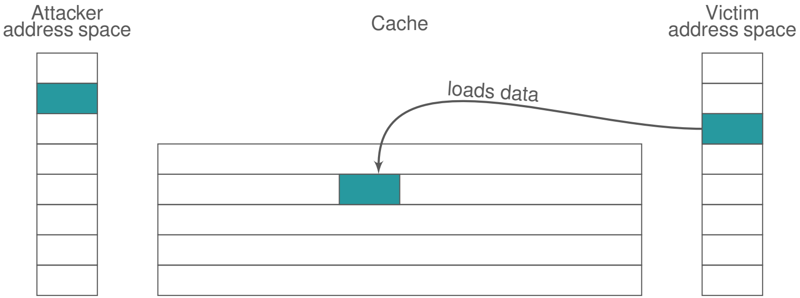

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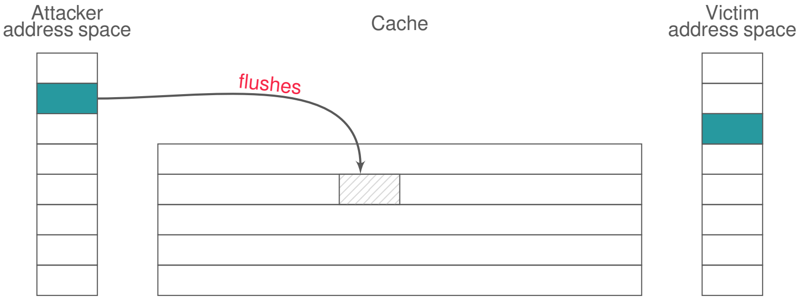

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step 3: attacker flushes data → high execution time if the victim loaded the line

Flush+Reload vs. Flush+Flush

Flush+Reload spy

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Victim

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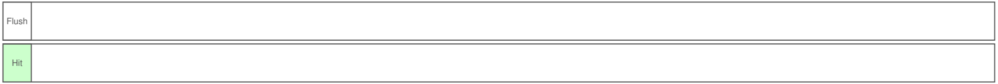

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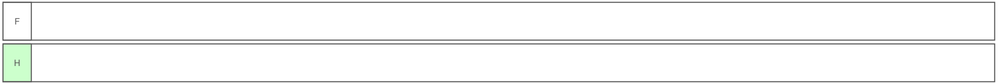

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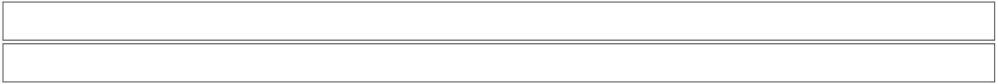

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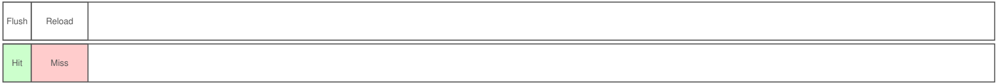

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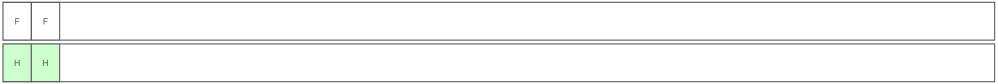

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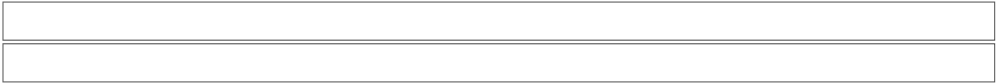

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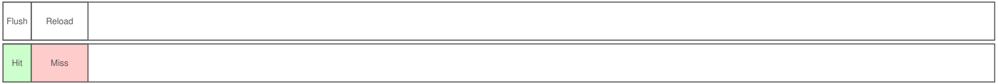

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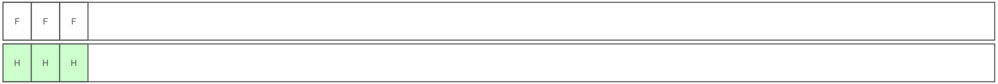

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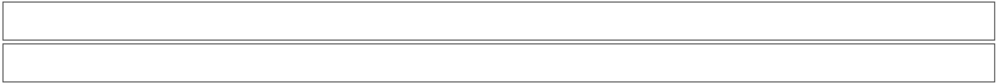

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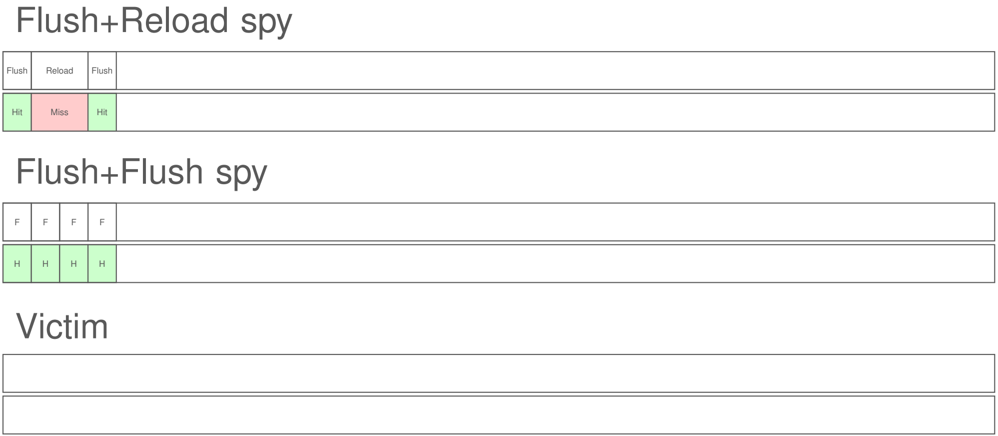

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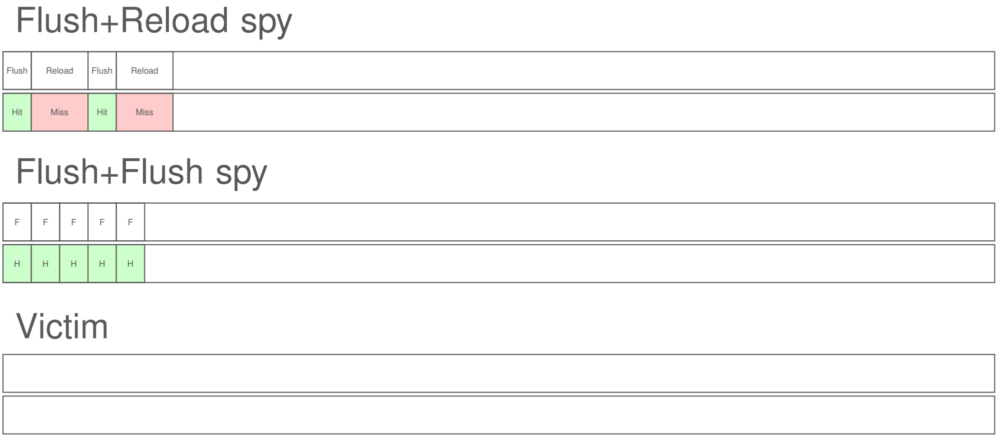

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Flush+Reload spy

Flush	Reload	Flush	Reload	
Hit	Miss	Hit	Miss	

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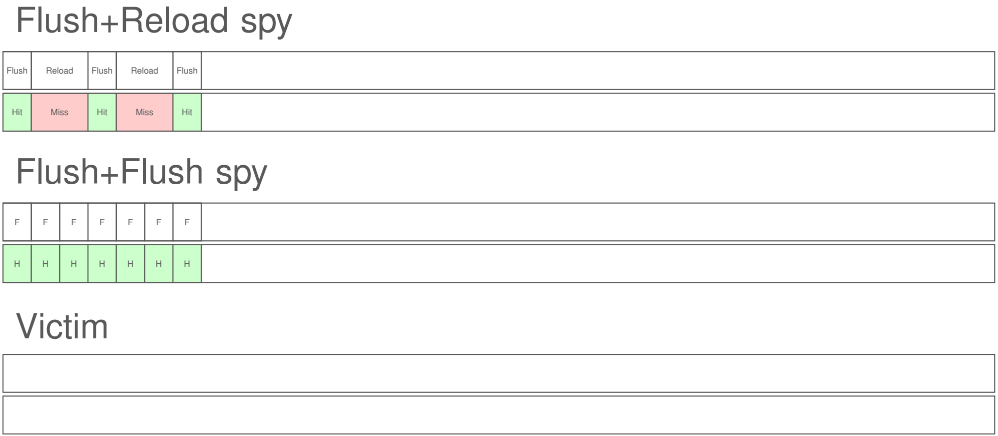

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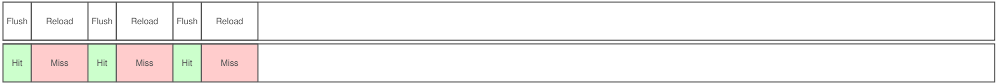

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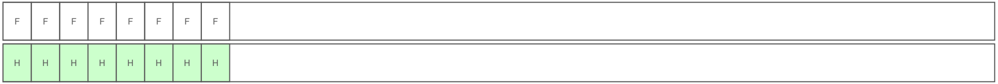

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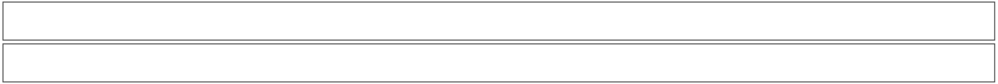

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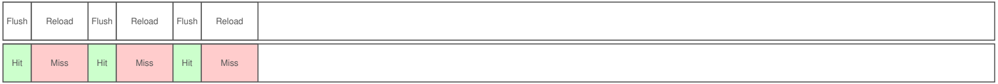

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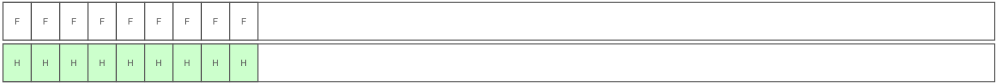

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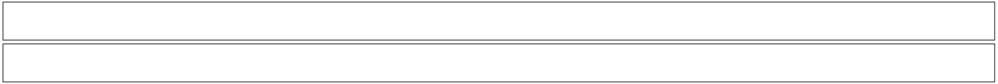

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Flush	Reload	Flush	Reload	Flush	Reload	Flush	
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Flush+Flush spy

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H	H	H	H	H	H	H	H	H	H	

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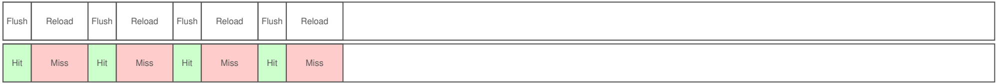

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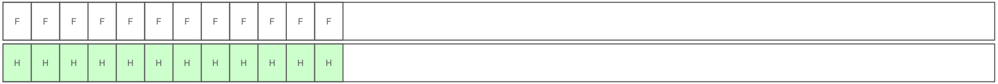
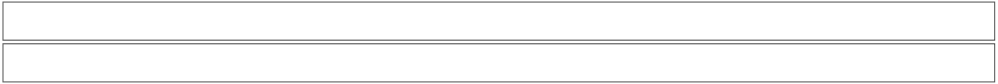
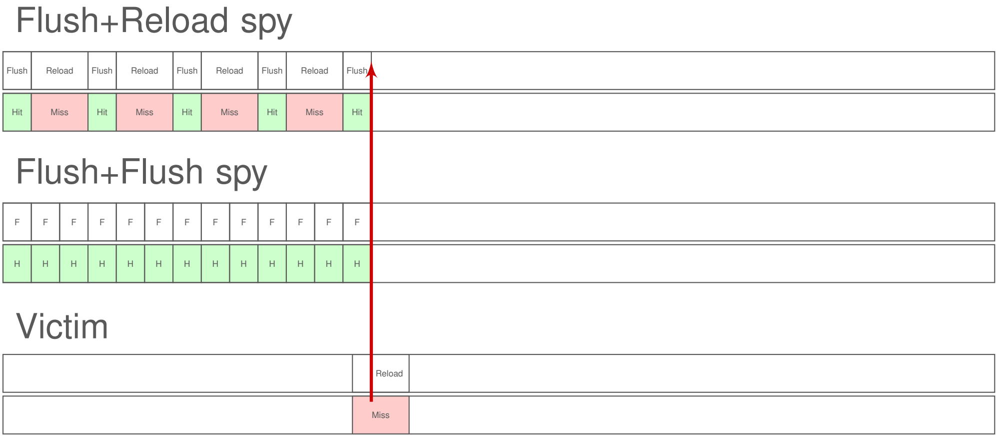


Victim



Flush+Reload vs. Flush+Flush



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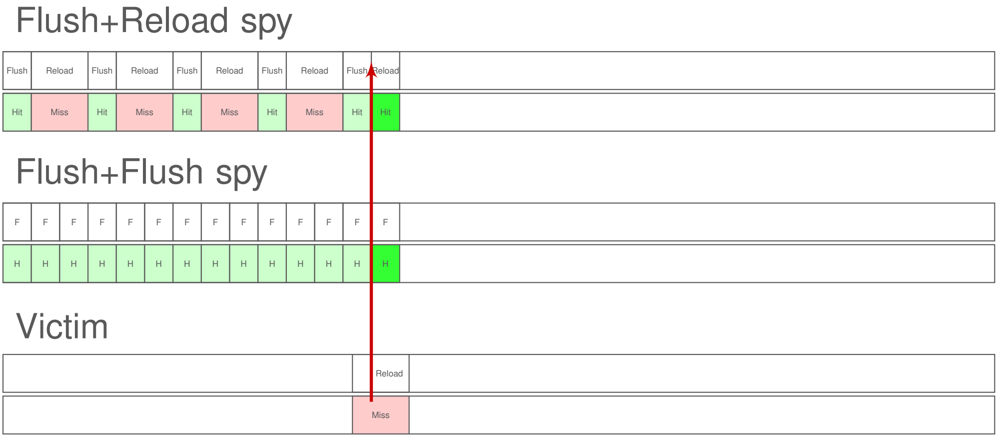

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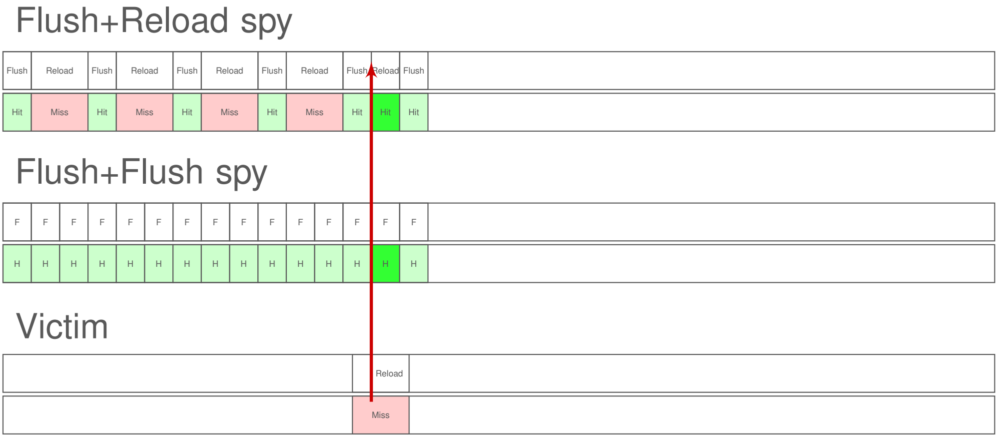

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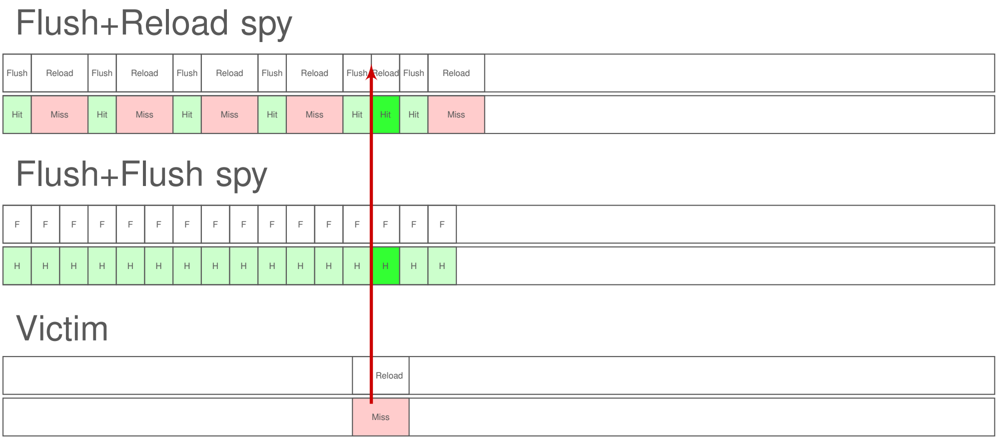

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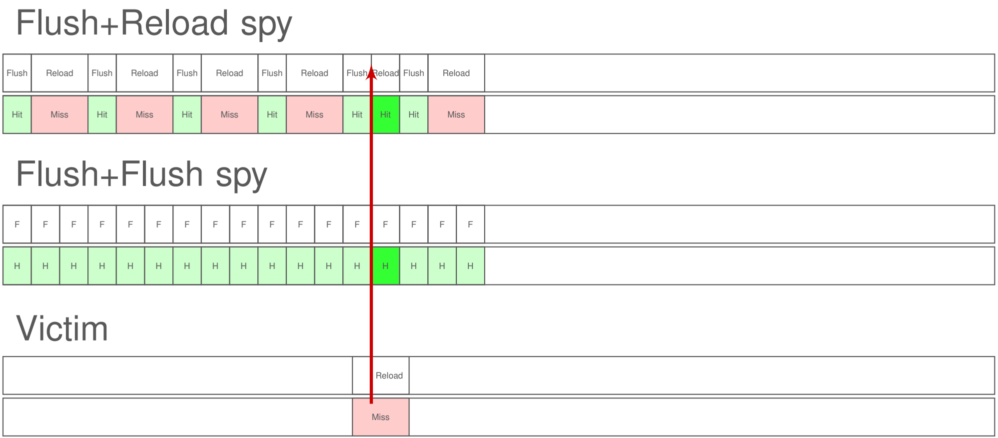

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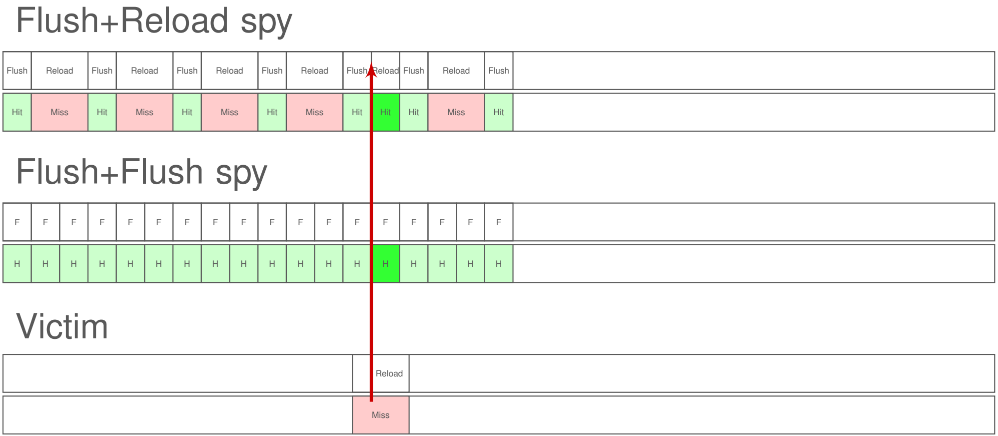

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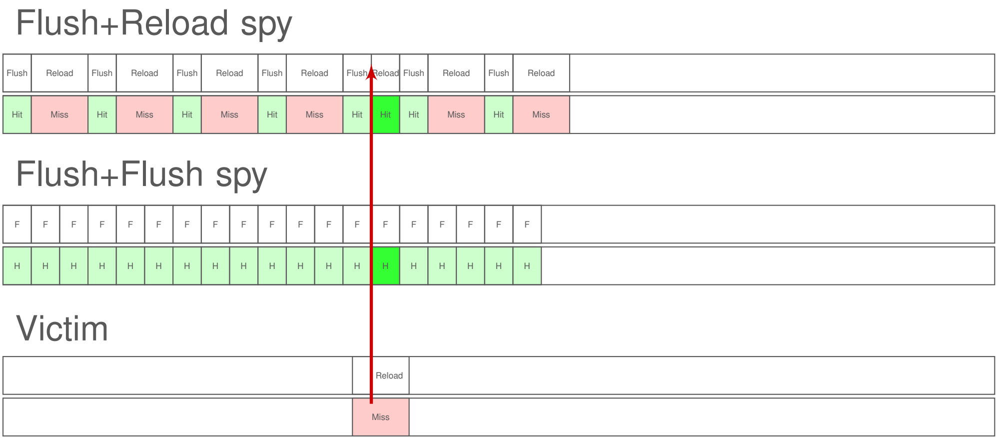

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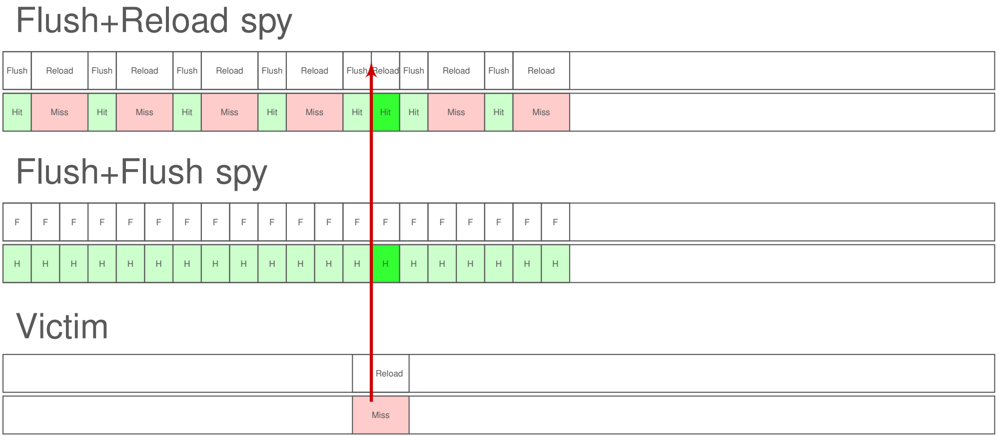

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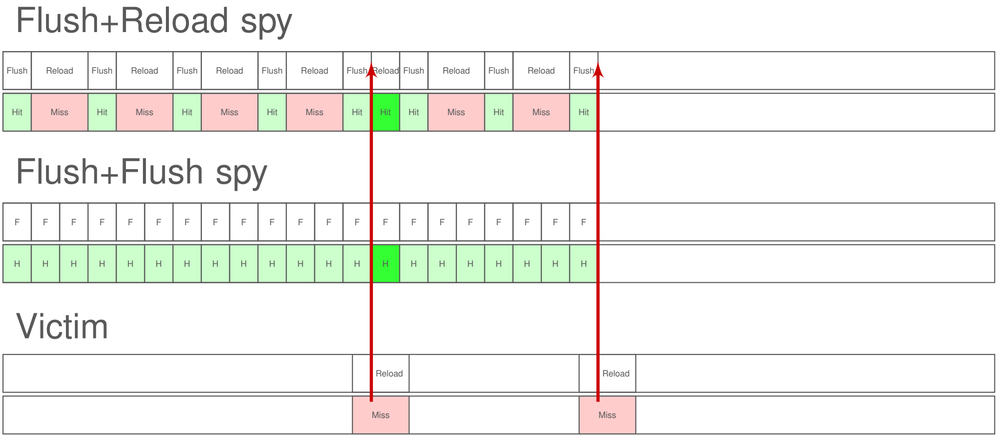

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Flush+Reload vs. Flush+Flush

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Flush+Flush: Covert channel

technique	packet size	capacity (KBps)	receiver stealth	sender stealth
Flush+Flush	28			
Flush+Reload	28			

Flush+Flush: Covert channel

technique	packet size	capacity (KBps)	receiver stealth	sender stealth
Flush+Flush	28	496		
Flush+Reload	28	298		

Flush+Flush: Covert channel

technique	packet size	capacity (KBps)	receiver stealth	sender stealth
Flush+Flush	28	496	✓	
Flush+Reload	28	298	✗	

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technique	packet size	capacity (KBps)	receiver stealth	sender stealth
Flush+Flush	28	496	✓	✗
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Flush+Flush	28	496	✓	✗
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Flush+Flush: Covert channel

technique	packet size	capacity (KBps)	receiver stealth	sender stealth
Flush+Flush	28	496	✓	✗
Flush+Reload	28	298	✗	✗
Flush+Reload	4			
Flush+Flush	4			
Prime+Probe	4			

Flush+Flush: Covert channel

technique	packet size	capacity (KBps)	receiver stealth	sender stealth
Flush+Flush	28	496	✓	✗
Flush+Reload	28	298	✗	✗
Flush+Reload	4	54		
Flush+Flush	4	52		
Prime+Probe	4	34		

Flush+Flush: Covert channel

technique	packet size	capacity (KBps)	receiver stealth	sender stealth
Flush+Flush	28	496	✓	✗
Flush+Reload	28	298	✗	✗
Flush+Reload	4	54	✗	
Flush+Flush	4	52	✓	
Prime+Probe	4	34	✗	

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technique	packet size	capacity (KBps)	receiver stealth	sender stealth
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Flush+Reload	4	54	✗	✓
Flush+Flush	4	52	✓	✓
Prime+Probe	4	34	✗	✗

Flush+Flush: Covert channel

technique	packet size	capacity (KBps)	receiver stealth	sender stealth
Flush+Flush	28	496	✓	✗
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Flush+Reload	4	54	✗	✓
Flush+Flush	4	52	✓	✓
Prime+Probe	4	34	✗	✗

Flush+Flush: Side channel on AES T-tables (1)

Number of encryptions to determine the upper 4 bits of a key byte

technique	number of encryptions
Flush+Reload	250
Flush+Flush	350
Prime+Probe	4 800

→ same performance for Flush+Flush and Flush+Reload

Flush+Flush: Side channel on AES T-tables (2)

Stealth comparison on 256 million encryptions

technique	time (s)	stealth
Flush+Reload	215	✗
Prime+Probe	234	✗
Flush+Flush	163	✓

→ Flush+Flush is the only stealthy spy process
→ others need to be slowed down too much to be practical

Countermeasures

- `clflush`
  - unprivileged line eviction

Countermeasures

- `clflush`
  - unprivileged line eviction → make it privileged

Countermeasures

- `clflush`
    - unprivileged line eviction $\rightarrow$ make it privileged
    - leaks timing information

Countermeasures

- `clflush`
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Countermeasures

- `clflush`
  - unprivileged line eviction → make it privileged
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- `rdtsc`
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  - fine-grained timing

Countermeasures

- `clflush`
  - unprivileged line eviction → make it privileged
  - leaks timing information → make it constant-time
- `rdtsc`
  - unprivileged timing → make it privileged
  - fine-grained timing → make it coarse-grained

Countermeasures

- `clflush`
  - unprivileged line eviction $\rightarrow$ make it privileged
  - leaks timing information $\rightarrow$ make it constant-time
- `rdtsc`
  - unprivileged timing $\rightarrow$ make it privileged
  - fine-grained timing $\rightarrow$ make it coarse-grained
- disable shared memory

1. Introduction

2. Flush+Flush

3. Conclusion and future work

Conclusion and future work

- `clflush` leaks enough information to enable a side channel
- Flush+Flush is a novel cache attack that makes no memory access

  → faster and stealthier than previous cache attacks

Conclusion and future work

- `clflush` leaks enough information to enable a side channel
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  $\rightarrow$ faster and stealthier than previous cache attacks

Future work

- new detection mechanism
- exploit timing difference of slices

Flush+Flush: A Fast and Stealthy Cache Attack

Daniel Gruss, Clémentine Maurice, Klaus Wagner and Stefan Mangard
Graz University of Technology

July 8, 2016 — DIMVA 2016

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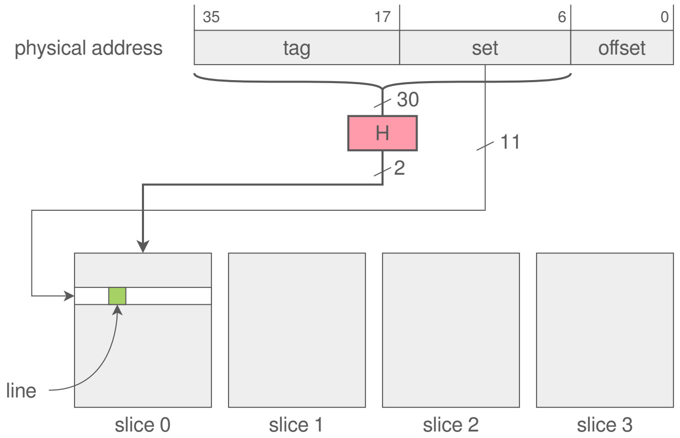
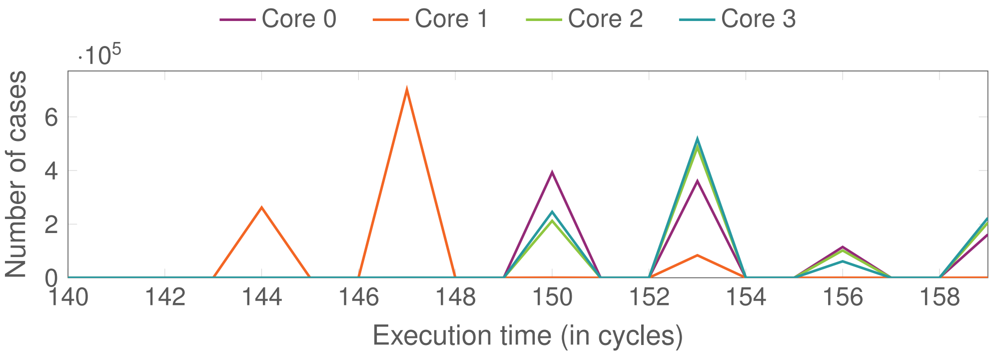
Last-level cache addressing



Bonus: Even more timing leakage



Performance counters: Usages

- answers “what’s happening in the system?”
- performance tuning $\rightarrow$ find bottlenecks
- side-channels [BM15]
- reverse-engineering microarchitecture [MLSNHF15]
- attack detection [DMSTWSS13; HF15; Pay16]